ABOUT THE INSTITUTE

Mahatma Gandhi Institute Of Technology (MGIT) was established by the Chaitanya Bharathi Educational Society (CBES) in 1997 and since inception it maintained good academic track record and stood among the top engineering colleges in Andhra Pradesh and Telangana. The primary objective of this society is to create temples of knowledge so as to impart value-based education to the present and future generations of our country. MGIT is permanently affiliated to JNTU, Hyderabad and Accredited by NAAC with 'A' Grade and also accredited three times by National Board of Accreditation (**NBA**), IEI and also recognized by UGC under 2(f) and 12(b). The college offers UG Programmes in eight branches of Engineering with a total intake of 900 (ECE, CSE, EEE, IT, MCT, MEC, Civil and MMT) and six branches of PG with a total intake of 108.

MGIT has well qualified faculty members with 52 Ph.D holders, 70 faculty members registered for Ph.D with reputed Institutions and 163 qualified non teaching staff. The Institution was ranked among the best Engineering Colleges in the band of 150-200 by NIRF, MHRD in the year 2017. CSR-GHRDC rated MGIT as one of the top emerging engineering colleges of excellence from A.P. and Telangana at all India level. The **Week Magazine** has rated MGIT among top 100 engineering colleges in India. **ISTE chapter** of MGIT has been adjudged as the best chapter of A.P. for the year 2012. AICTE has funded the IIPC, RPS and EDC, MODROBS projects and also sanctioned grant in aid for organizing FDP Programs. Many reputed Multinational companies are regularly visiting MGIT for campus placements.

ABOUT THE DEPARTMENT

The department of Electronics & Communication Engineering was started in the year 2000 with a vision to mould competent Electronics and Communication engineers with sound theoretical and practical knowledge, working for the betterment of Humankind. The department has excellent infrastructure facilities, laboratories and Department has forty well experienced & qualified faculty supported by dedicated technical staff. The Department has R&D and project lab. The department has successfully completed AICTE sanctioned research project (RPS) & FDP. The department of Electronics & Communication Engineering regularly organizes National level technical events and seminars.

ABOUT THE FDP

The field of VLSI design has an enormous growth in the research over the past two decades. This course is aimed and designed to provide a better hands on experience for the participants in using the Front end & Backend design tools of VLSI such as Xilinx & Mentor Graphics.

COURSE CONTENT

- **Overview of ASIC/FPGA design and its Applications**
- **Full Custom & Semi Custom design flow**
- **Physical Verification using Industry Standard Calibre Tool**
- **Designing Hardware using ZYNQ SOC**
- **Hands on Sessions for Front end & Back end VLSI design using Xilinx ISE, VIVADO & Mentor Graphics**
- **Research applications in VLSI Design**

RESOURCE PERSONS

The course lectures will be delivered by the faculty members, scientists and industrial experts from the reputed institutions such as APPLY VOLT , CoreEL, DRDL, and Premier Academic Institutions like IIITH, IIT, JNTUH and many more eminent speakers from R&D centers in the area of VLSI Design.

COURSE MATERIAL

Each participant will be provided with the course material and lecture notes.

NATIONAL LEVEL ONE WEEK
FACULTY DEVELOPMENT PROGRAMME (FDP)
ON

"E-CAD & VLSI DESIGN"

8-12 JULY, 2019

Organized by
DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING
MAHATMA GANDHI INSTITUTE OF TECHNOLOGY
Gandipet, Hyderabad. Telangana, 500 075
www.mgit.ac.in

REGISTRATION FORM

1. Name (Block Letters) :
2. Designation :
3. Organization :
4. Address for Correspondence :

5. Tel: (O) (M)
   E-mail:
6. Academic Qualification (Please Tick):
   M.Tech ( ) Ph.D ( )
7. Specialization:
8. Experience (in years):
   Teaching ( ) Industrial ( ) Research ( )
9. Gender: Male ( ) Female ( )

Please register me for the course **"E-CAD & VLSI DESIGN"** to be held at **MGIT, Hyderabad** during **8 -12 JULY, 2019.**

Date: Signature of the Applicant

DECLARATION

The information furnished above is true to the best of my knowledge. I agree to abide by the rules and regulations governing the course. If selected, I shall attend the course for entire duration; I also undertake the responsibility to inform the coordinator sufficiently in advance, in case I am unable to attend the course. On provisional selection, I will submit the registration fee on or before **29-06-2019**

Place:
Date:

Signature of the applicant

SPONSORSHIP CERTIFICATE

Certified that Dr/Mr/Ms_____
is an employee of our institute and is hereby sponsored for the One Week FDP on **"E-CAD & VLSI DESIGN"** at MGIT, Hyderabad to be held during the period **8 –12 July, 2019**. Our institute is approved by AICTE. He / She will be permitted to attend the FDP, if selected.

Place : **Signature of the Sponsoring Authority**
Date: **with seal**

The duly sponsored application should be mailed to:

Mr. D.V.S.Nagendra Kumar

Coordinator, FDP
Department of Electronics & Communication Engineering
Mahatma Gandhi Institute of Technology
Chaitanya Bharathi (post)
Gandipet, Hyderabad, Telangana- 500 075
Email: fdpece@mgit.ac.in
09849953764, 08466997012

APPLY VOLT- Ramesh Naidu-+91-9000900485

PATRONS

Sri P Prabhakar Reddy, Chairman, CBES

Kavikireeti' **Dr. V Malakonda Reddy,** Advisor, MGIT & President, CBIT

Sri N. Subash, Secretary, CBES

'Smt. D Sandhya Sree, Chairperson, Development & Purchase

ORGANISING COMMITTEE

Chairman
Dr. K. Jaya Sankar, Principal, MGIT

Vice Chairman
Dr. S.P.Singh, Professor & Head, ECE

Coordinator
Mr. D.V.S.Nagendra Kumar, Sr.Asst.Professor
Dept. of Electronics & Communication Engineering

Members
Faculty & Non – Teaching Staff of the Department

ELIGIBILTY

- The course is open to Engineering faculty & Research Scholars. A Registration fee of Rs. 1000/- has to be sent by the provisionally selected participants, in FDP.
- Participants from industries are also eligible to attend the FDP, with a course fee of Rs 3000/, towards Registration.
- The Registration fee can be paid through online payment as mentioned below.

Account Name: **MGIT RECURRING EXPENDITURE**
Account Number: **180401001260**
ICICI Bank, IFSC: **ICIC0001804**

IMPORTANT DATES

The number of delegates aimed for the program is limited. Selection of candidates is based on qualification and experience.

Last date for submission of filled in Registration form : **22nd June, 2019**
Intimation of Provisional Selection (By Email) : **29th June, 2019**
Last date of receipt of confirmation with registration fee: **06th July, 2019**
Considering postal delay, it is advised to send the scanned copy of registration form, duly counter signed by the Head of the Institution, by email to ***fdpece@mgit.ac.in***

APPLY VOLT

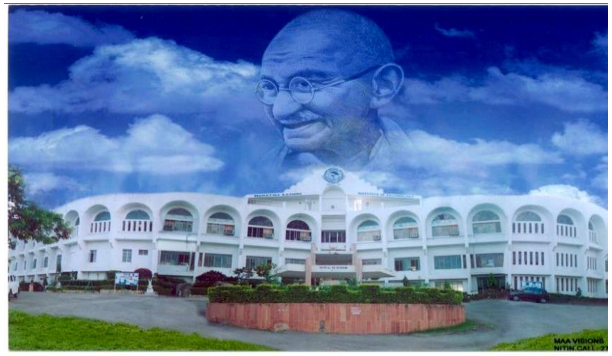
NATIONAL LEVEL ONE WEEK FACULTY DEVELOPMENT PROGRAMME (FDP)

ON

E-CAD & VLSI DESIGN

8-12 July, 2019

Coordinator
Mr. D.V.S.Nagendra Kumar



In association with

APPLY VOLT & CoreEL

Organized by

DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING

MAHATMA GANDHI INSTITUTE OF TECHNOLOGY

(ESTD IN 1997)
(Chaitanya Bharathi Educational Society)
NAAC Accredited with 'A' Grade, Permanently Affiliated to JNTUH, All UG Courses Accredited by NBA and Recognized under UGC 2(f) & 12 (b)
Gandipet, Hyderabad – 500 075
Phone: 09849953764, Fax: 040-24193067
FDP Email: fdpece@mgit.ac.in, www.mgit.ac.in