Code No: RR222201 **Set No. 1**

II B.Tech II Semester Regular Examinations, Apr/May 2006
SWITCHING THEORY AND LOGIC DESIGN
(Instrumentation & Control Engineering)

Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
All Questions carry equal marks

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1. (a) Decimal system became popular because we have 10 fingers. A rich person on earth has decided to distribute Rs. One lakh equally to the following persons from various planets. Find out the amount each one of them will get in their respective currencies.
   A from planet VENUS possessing 8 fingers
   B from plant MARS possessing 6 fingers
   C from planet JUPITER possessing 14 fingers
   D from plant MOON possessing 16 fingers
   (b) Write short notes on different types and properties of four bit codes with the aid of suitable examples.

   [8+8]

2. (a) Simplify the Boolean function F using the dont care conditions d, in
      i. sum of products and
      ii. product of sums where
      $F = \overline{A}\ \overline{B}\ \overline{D} + \overline{A}CD + \overline{A}BC$ *and* $d = \overline{A}B\overline{C}D + ACD + \overline{A}\ \overline{B}\ \overline{D}$
   (b) F(A, B, C, D) = π max [5, 8, 14] + d[7, 11, 12, 13, 15]. Obtain minimal sop function.

   [8+8]

3. (a) Derive Boolean expression for a 2input Ex-OR gate to realize with 2 input NAND gates without using complemented variables and draw the circuit.
   (b) Redraw the given circuit in (figure1)after simplification .

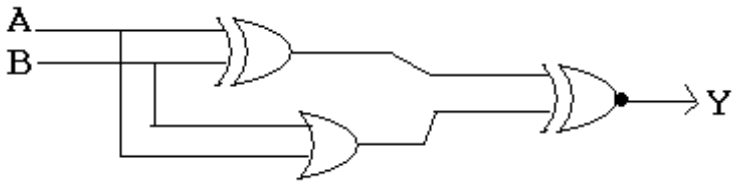

Figure 1:

[8+8]

4. (a) Write a note on 'display decoders'

(b) Design a 4 to 1 mux using a 2 to 4 decoder and basic gates.

[8+8]

5. (a) What is the race around condition in flip-flops. Explain with the help of example.

   (b) Give transition tables for the given flop-flops J-K, R-S, T and D-Flip-Flops

   (c) Draw the circuit of positive edge trigger J-K flip-flop with active high preset and active low clear and explain its operation with the help of Truth-Table.

[6+4+6]

6. Design the sequential circuit specified by the state diagram(figure2) using RS flipflops.

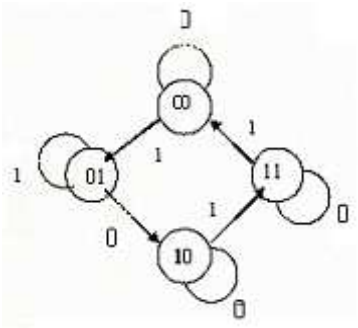

Figure 2:

[16]

7. For the machine shown in the table below obtain:

   (a) The corresponding reduced machine table in standard form

   (b) Find a minimum length that distinguishes state A from state B where PS: present state, NS: next state, Z: output, X: input

PS	NS,Z	
	X=0	X=1
A	B,1	H,1
B	F,1	D,1
C	D,0	E,1
D	C,0	F,1
E	D,1	C,1
F	C,1	C,1
G	C,1	D,1
H	C,0	A,1

[10+6]

8. Construct an ASM block that has 3 input variables (A,B,C), 4 output (W,X,Y,Z) and 2 exit paths. For this block, output Z is always 1, and W is 1 if A & B are both 1. If C=1 & A=0, Y=1 and exit path 1 is taken. If C=0 or A=1, X=1 and exit path 2 is taken. Realize the above using the multiplier and register. [16]

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Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
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1. (a) Perform the subtraction with the following unsigned binary numbers by taking the 2's complement of the subtrahend.
   i. 11010-10000
   ii. 11010-1101
   iii. 100-110000
   iv. 1010100-1010100
   (b) The binary numbers listed have a sign bit in the left most position and, if negative, are in 1's complement form. Perform the arithmetic operations indicated and verify the answers.
   i. 101011+111000
   ii. 001110+110010
   iii. 111001-001010
   iv. 101011-100110

[8+8]

2. (a) Find the minimal expression for the function f(w,x,y,z)=$\sum$(0,2,5,9,15) +$\sum$d (6,7,8,10,12,13) using Karnaughs-map.
   (b) i. Determine the Canonical sum-of-products form for $T(x, y, z) = \overline{x}y + \overline{z} + xyz$
   ii. Minimize the function $f(x, y, z, w) = x + xyz + wx + \overline{x}y + \overline{w}x + \overline{x}yz$.

[8+4+4]

3. (a) Derive Boolean expression for a 2 input Ex-NOR gate to realize with two input NOR gates, without using complemented variables and draw the circuit.
   (b) Redraw the given circuit (figure1) after simplification.

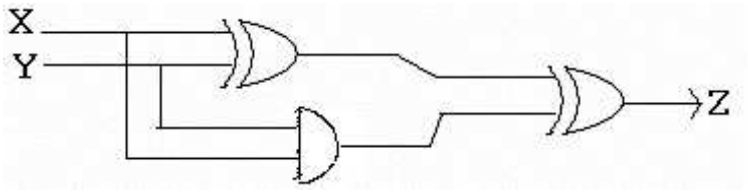

Figure 1:

[8+8]

4. (a) Design a combinational circuit that accepts a 3-bit number and generates an output binary number equal to the square of the input number.
   (b) Realize a 3-bit odd-parity generator circuit using only two-input ex-or gate

[8+8]

5. (a) Obtain the excitation table for the given flip-flops
      i. J-K-flip-flop
      ii. D-flip-flop
   (b) Draw the schematic circuit of S-R-Flip-Flop with negative edge triggering using NAND gates and explain its operation with proper truth-table. Convert this flip-flop to J-K flip-flop and explain its operation

[6+10]

6. Design a 4-bit universal shift register and draw the circuit with the given mode of operation table.

S_1	S_0	Operation
0	0	Parallel
0	1	Shift right
1	0	Shift left
1	1	Inhibit clock

[16]

7. For the machine shown in the table below obtain:
   (a) The corresponding reduced machine table in standard form
   (b) Find a minimum length that distinguishes state A from state B where PS: present state, NS: next state, Z: output, X: input

PS	NS,Z	
	X=0	X=1
A	B,1	H,1
B	F,1	D,1
C	D,0	E,1
D	C,0	F,1
E	D,1	C,1
F	C,1	C,1
G	C,1	D,1
H	C,0	A,1

[10+6]

8. (a) Draw the state diagram and the state table of the control unit conditions given below. Draw the equivalent ASM chart leaving the state box empty.
      i. from 00 state, if x = 1 , it goes to 01 state and if x = 0, it remains in the same state 00.
      ii. from 01 state, if y = 1, it goes to 11 state and if y = 0, it goes to 10 state.

iii. from 10 stae, if x = 1 and y = 0, it remains in the same state 10 and if x = 1 and y = 1, it goes to 11 state, and if x = 0, it goes to 00 state.

iv. from 11 state, if x = 1, y = 0, it goes to 10 state and if x = 1, and y = 1, it remains in the same state, and if x = 0, it goes to 00 state.

(b) Design the control using PLA and register.for the above problem.

[8+8]

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Code No: RR222201 **Set No. 3**

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Time: 3 hours **Max Marks: 80**

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1. (a) Convert the following numbers to be indicated bases.
   i. 7562.45 to octal
   ii. 1938.257 to hexadecimal
   (b) Add and multiply the following numbers without converting to decimal
   i. $(367)_8$ and $(715)_8$
   ii. $(15F)_{16}$ and $(A7)_{16}$
   (c) Add in BCD form (98) and (87).

   [4+8+4]

2. (a) Find the minimal expression for the function f(w,x,y,z)=$\sum$(0,2,5,9,15) +$\sum$d (6,7,8,10,12,13) using Karnaughs-map.
   (b) i. Determine the Canonical sum-of-products form for $T(x, y, z) = \overline{x}y + \overline{z} + xyz$
   ii. Minimize the function $f(x, y, z, w) = x + xyz + wx + \overline{x}y + \overline{w}x + \overline{x}yz$.

   [8+4+4]

3. (a) Implement the following function using only NOR gates F=a .(b+ c.d) + (b . $\overline{c}$).
   (b) Implement the following function using only NAND gates G=(a + $\overline{b}$). (c. d + $\overline{e}$)
   (c) Give the minimum two-level SOP realization of the following switching function using only NAND gates. F(x,y,z) = $\sum$ m (0,3,4,5,7)

   [4+4+8]

4. (a) Design a combinational circuit that accepts a 3-bit number and generates an output binary number equal to the square of the input number.
   (b) Realize a 3-bit odd-parity generator circuit using only two-input ex-or gate

   [8+8]

5. (a) With the help of block-diagrams, explain the difference between synchronous sequential circuit and Asynchronous sequential circuit and compare them.
   (b) For the block diagram(figure1) shown below, draw the schematic circuit using NAND gates and explain its working with the help of Truth-Table.

   [6+10]

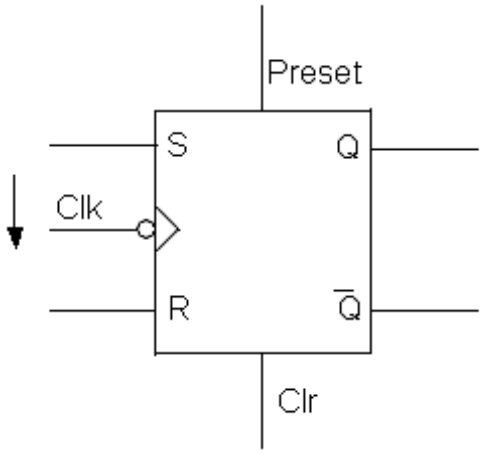

Figure 1:

6. Derive the state diagram and state table for two input(x_1, x_2) and single output z asynchronous circuit. The output of the circuit $z = x_1$ if $x_2 = 1$, but if $x_2 = 0$, the output is to remain fixed at its last value before x_2 becomes zero and design the circuit using D-flip flops. [16]

7. For the machine shown in the table below obtain:

   (a) The corresponding reduced machine table in standard form

   (b) Find a minimum length that distinguishes state A from state B where PS: present state, NS: next state, Z: output, X: input

PS	NS,Z	
	X=0	X=1
A	B,1	H,1
B	F,1	D,1
C	D,0	E,1
D	C,0	F,1
E	D,1	C,1
F	C,1	C,1
G	C,1	D,1
H	C,0	A,1

[10+6]

8. Obtain the ASM charts for the following state transition

   (a) If x = 0, control goes from T1 to state T2, if x = 1, generate the conditional operation and go from T1 to T2.

   (b) If x = 1, control goes from T1 to T2 and then to T3, if x = 0, control goes from T1 to T3.

   (c) Start from state T1, then if xy = 00, go to T2, if xy = 01, then go to T3, if xy = 10, then go to T1, otherwise go to T3. and design its control circuit using

i. D flip flop & decoder
ii. Input multiplexer & a register

[8+8]

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Code No: RR222201 **Set No. 4**

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Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
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1. (a) Consider the following four codes.

Code A		Code B		Code C		Code D	
0001		000		01011		000000	
0010		001		01100		001111	
0100	2	011	1	10010	3	110011	4
1000		010		10101			
		110					
		111					
		101					
		100					

Which of the following properties is satisfied by each of the above codes?

i. Detects single errors
ii. Detects double errors
iii. Detects triple errors
iv. Corrects single errors
v. Corrects double errors
Corrects singe and detects double errors.

(b) Add the following decimal number 109 and 876 in BCD and Excess-3 forms.

[8+8]

2. (a) With the use of maps find the simplest form in sum of products of the function F =fg. where f and g are given by
$f = wx\overline{y} + \overline{y}z + \overline{w}y\overline{z} + \overline{x}y\overline{z}$
$g = (w + x + \overline{y}\ \overline{z})(\overline{x} + \overline{y} + z)(\overline{w} + y + \overline{z})$

(b) Obtain the simplified expression in POS (product of sums) of F(w,x,y,z) =π(1,3,5,7,13,15)+d(6, 12, 14)

[8+8]

3. Using the tabular method, obtain the prime implicants of a four- input single-output function f(w,x,y,z) = $\sum$m(0,2,4,5,6,7,8,9,10,11,13). Reduce the prime-implicant table and find the minimal cover of f. [16]

4. (a) Design a full-adder with two half-adders and basic gates.

(b) Convert Excess-3 code to BCD using Full adder circuits.

[8+8]

5. (a) Define the following systems
   i. synchronous sequential system
   ii. asynchronous sequential system
   iii. combinational system
   (b) Draw the schematic circuit of a negative edge triggered D-Flip-Flop using NAND gates and give its truth-table. Justify the entries in the truth-table.

   [6+101]

6. Design a sequential circuit with two D flipflops A and B and one input x. When x=0, the state of the circuit remains the same. When x=1, the circuit goes through the state transitions from 00 to 01 to 11 to 10 back to 00 and repeats. [16]

7. For the machine given below, find the equivalence partition and a corresponding reduced machine in standard form and also explain the procedure:

PS	NS,Z	
	X=0	X=1
A	B,0	E,0
B	E,0	D,0
C	D,1	A,0
D	C,1	E,0
E	B,0	D,0

   [16]

8. Construct an ASM block that has 3 input variables (D,E,F) and 4 output variables (P,Q,R,S) and 2 exit paths. For this block, output P is always 1, and Q is 1 if D=1. If D & F are 1 or if D & E are 0, R=1 and exit path 2 is taken. If (D=0 & E=1) or (D=1 & F=0), S=1 and exit path 1 is taken.
   Realize it with One flip flop per state. [16]

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