Code No: NR220203 **NR**

II B.Tech II Semester Supplementary Examinations, Apr/May 2006
LINEAR & DIGITAL IC APPLICATIONS
(Common to Electrical & Electronic Engineering and Electronics & Computer Engineering)

Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
All Questions carry equal marks

⋆ ⋆ ⋆ ⋆ ⋆

1. (a) Derive the expression for CMRR for the first stage differential amplifier [8]
   (b) Explain about any two linear and nonlinear applications of OP-AMP [8]

2. (a) Design a unity gain summing amplifier to add three dc input voltages -0.5V, 0.1V and 0.75V in inverting configuration. If the saturation voltages of the OP-AMP are +18V, and -18V, find the possible maximum gain of the amplifier. [8]
   (b) Design a subtractor circuit whose output is equal to the difference between the two inputs. Use a differential OP-AMP configuration [8]

3. (a) Design a saw tooth wave form generator using OP-AMP and plot the waveforms for the given specifications frequency: 5KHz, $V_{sat} = \pm 15V$ (Assume necessary data) [8]
   (b) What is the difference between a basic comparator and the Schmitt trigger? Construct a Schmitt trigger circuit using OP-AMP and derive the threshold voltages. [8]

4. (a) Explain the operation of Monostable multivibrator using 555 timer. Derive the expression of time delay of a Monostable multivibrator using 555 timer. [10]
   (b) Design a Monostable multivibrator using 555 timer to produce a pulse width of 100 m sec. [6]

5. (a) Explain the terms Lock range, Capture range and Pull-in time a PLL. How are Lock Range and Capture range determined? [8]
   (b) Design a PLL circuit using IC 565 to get
      i. Free-running frequency = 4.5 KHz
      ii. Lock range of 2 KHz and
      iii. Capture range = 100 Hz.

      Assume a supply voltage of + or - 10V. Show the circuit diagram with all component values. [8]

6. (a) Define Bessel, Butterworth and Chebysher filters, and compare their frequency response. [8]
   (b) Sketch the circuit diagram of band elimination filter and design a wide band-reject having f_H=200Hz and f_L=1kHz. Assume necessary data. [8]

7. (a) What is meant by AOI Logic. Explain with the help of example. [6]
   (b) Draw the circuit of an improved version of D.T.L. 3-input Nand gate, and explain its operations with the help of Truth Table If h_{FE} of each transistor is 40, find FAN-OUT of the circuit. [10]

8. (a) What is a sample-and-hold circuit? Draw the circuit diagram and explain its action? [6]
   (b) With reference to sample and hold circuit define the following terms: [4]
      i. Aperture time
      ii. Hold mode.
   (c) Draw the circuit of Weighted Resistor DAC and derive expression for output analog voltage V_o. [6]

⋆ ⋆ ⋆ ⋆ ⋆