Code No: RR321202 **Set No. 1**

III B.Tech II Semester Regular Examinations, Apr/May 2006
VLSI SYSTEMS DESIGN
(Information Technology)

Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
All Questions carry equal marks

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1. Implement the following gates with n-MOS transistors only and explain its working
   (a) 3 Input NAND gate.
   (b) Inverter. [8+8]
2. Explain working principal of n-MOS transistor with sketches of its structure. [16]
3. Design a stick diagram for CMOS logic shown below.
   $Y = (AB + CD)^1$ [16]
4. Design a layout for CMOS 3-input NOR gate. [16]
5. Explain the delay calculation procedure for CMOS inverter. [16]
6. Draw the structure of carry select adder and explain its working principle. [16]
7. Explain how Architecture driven voltage scaling technique reduces the power consumption of the design. [16]
8. Clearly explain about event driven simulation with suitable example. [16]

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Code No: RR321202 **Set No. 2**

III B.Tech II Semester Regular Examinations, Apr/May 2006
VLSI SYSTEMS DESIGN
(Information Technology)

Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
All Questions carry equal marks

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1. Implement the following logic functions using CMOS logic
   (a) $Y = \{A.B.C.D\}^1$
   (b) $Y = \{A + B + C + D\}^1$ [8+8]
2. An n-MOS transistor is operating in the triode region with the following parameters $\mu_n Cox = 90\mu\ A/V^2$ W/L (ratio) = 100 $Vgs = 4V$, $V_{tn} = 1V$, $V_{ds} = 2V$. Find its drain current & drain -Source resistance. [16]
3. Design a stick diagram for CMOS EX-NOR gate. [16]
4. (a) What do you mean by layout of a component?
   (b) Draw neat layout diagram for NMOS transistor [8+8]
5. Define faults of a Digital circuit and Explain about struck at 0 /1 faulty models [16]
6. Give a complete table of the barrel shifter's possible operations. List all possible combinations of top and bottom inputs and the resulting operation. [16]
7. Clearly discuss about power distribution and clock distribution routing procedure. [16]
8. Sketch the architecture of the kitchen timer chip and explain about its architecture design. [16]

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Code No: RR321202 **Set No. 3**

III B.Tech II Semester Regular Examinations, Apr/May 2006
VLSI SYSTEMS DESIGN
(Information Technology)

Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
All Questions carry equal marks

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1. Implement the following logic functions using CMOS logic
   (a) $Y = \{(A + B)(C + D)\}^1$
   (b) $Y = \{AB + C\}^1$ [8+8]
2. Explain about different computer aided design tools used in designing Integrated Circuits. [16]
3. Explain with neat sketches CMOS fabrication using P - well process. [16]
4. (a) What do you mean by layout of a component?
   (b) Draw neat layout diagram for NMOS transistor [8+8]
5. Define faults of a Digital circuit and Explain about struck at 0 /1 faulty models [16]
6. Draw the structure of carry select adder and explain its working principle. [16]
7. Clearly explain how ASM chart is a useful abstraction for register transfer design. [16]
8. With suitable example explain any one of the scheduling algorithm [16]

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Code No: RR321202 **Set No. 4**

III B.Tech II Semester Regular Examinations, Apr/May 2006
VLSI SYSTEMS DESIGN
(Information Technology)

Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
All Questions carry equal marks

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1. Implement the following gates with CMOS Logic and explain its working
   (a) 2 Input NAND gate.
   (b) 3 Input NOR gate. [8+8]
2. Name different IC fabrication technologies with suitable examples. [16]
3. Design a stick diagram for CMOS, EX-OR and Inverter gates. [16]
4. Implement EX-OR and EX-NOR gates using static complementary logic. [16]
5. (a) Explain the power calculation procedure of CMOS inverter.
   (b) Explain the speed - power product significance of a logic family. [8+8]
6. Discuss clearly about the following system Design principles.
   (a) Pipelining
   (b) Data-paths [8+8]
7. Explain clearly the detailed routing phase of the floor planning of the chip with few examples by considering all constraints. [16]
8. Sketch the architecture of the kitchen timer chip and explain about its architecture design. [16]

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