Code No: RR321301 **Set No. 1**

III B.Tech II Semester Regular Examinations, Apr/May 2006
COMPUTER ORGANIZATION
(Electronics & Control Engineering)

Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
All Questions carry equal marks

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1. (a) List the types of transfers supported by interconnection structure.
   (b) Discuss the reasons for undermining bus performance
   (c) Explain various bus configuration examples. [5+5+6]
2. (a) Explain about booth coding
   (b) Find the booth coded numbers of the following binary numbers
      i. 01101111101
      ii. 000111110110 [8+8]
3. Explain various characteristics of machine instructions in detail [16]
4. Elaborate on different types of registers in a register organization [16]
5. (a) Discuss the principles of associative memory.
   (b) Explain the functioning of 4 x 4 bit associative memory array.
   (c) Explain the cache with two-way set-associative addressing [6+4+6]
6. (a) Explain how bus arbitration is done in DMA transfer
   (b) Discuss about the generic model of an I/O module. [8+8]
7. (a) Discuss about I/O channel architecture.
   (b) Discuss about I/O addressing in 8086.
   (c) Discuss the salient features of laser printer [6+6+4]
8. (a) Why special handling is required for branch instruction in a pipelined processor. Explain with examples.
   (b) How would you determine the number of pipeline stages in a pipelined processor [10+6]

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Code No: RR321301 **Set No. 2**

III B.Tech II Semester Regular Examinations, Apr/May 2006
COMPUTER ORGANIZATION
(Electronics & Control Engineering)

Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
All Questions carry equal marks

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1. (a) How mandatory signal lines for PCI are functionally grouped
   (b) Explain typical desktop system using PCI configuration. [8+8]

2. (a) Find the output binary number after performing the following arithmetic operations
      i. 111.01 + 10.111
      ii. 11.01 + 110.11
      iii. 110.11 - 111.01
   (b) Explain about the longhand division of binary integers. [6+10]

3. NOOP instruction has no effect on the CPU state other than incrementing the program counter. Suggest some uses of this instruction with examples. [16]

4. (a) Differentiate between interrupts and exceptions.
   (b) What do you mean by interrupt vector table?
   (c) Write about Pentium exception and interrupt vector table. [5+5+6]

5. (a) Explain different techniques of cache mapping function
   (b) what are the merits and demerits of each. [10+6]

6. (a) Explain about CD-ROM block format.
   (b) What is WORM? Also explain its uses.
   (c) Differentiate between disk layout using constant angular velocity and constant linear velocity [5+5+6]

7. (a) How the address of next microinstruction is known while executing a micro program.
   (b) Discuss about branch control logic in microinstruction sequencing with variable address format. [6+10]

8. (a) Explain about directory protocols.
   (b) Draw and explain the state diagram for MESI protocol. [6+10]

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Code No: RR321301 **Set No. 3**

III B.Tech II Semester Regular Examinations, Apr/May 2006
COMPUTER ORGANIZATION
(Electronics & Control Engineering)

Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
All Questions carry equal marks

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1. (a) Differentiate between dedicated and multiplexed bus lines.
   (b) Discuss various methods of bus arbitration.
   (c) What do you mean by bus width? [5+7+4]
2. (a) Find the output of the following binary expressions using 2's complement representation.
      i. 111.01 + 10.111
      ii. 110.11 - 111.01
   (b) Explain the steps involved in the subtraction of a number from a given number using 1's complement notation [10+6]
3. Explain various characteristics of machine instructions in detail [16]
4. (a) List and describe various co-processor and special instructions of MIPS R-series processors.
   (b) Differentiate between theoretical R3000 and actual R4000 super pipelines. [10+6]
5. (a) Explain the cache execution of a read operation with a neat diagram
   (b) Explain look-aside system organization for caches. [8+8]
6. (a) What is multiple-platter disk.
   (b) Differentiate between fixed and movable head disks.
   (c) Define 'disk access time', 'seek time' and 'rotational latency'. [5+5+6]
7. (a) Discuss about the evolution of I/O function.
   (b) Explain the characteristics of I/O channels. [8+8]
8. (a) Discuss about exeception in multiple execution unit pipelined processors with examples.
   (b) Discuss about dispatch and superscalar operation in multiple execution unit pipelined processors [8+8]

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Code No: RR321301 **Set No. 4**

III B.Tech II Semester Regular Examinations, Apr/May 2006
COMPUTER ORGANIZATION
(Electronics & Control Engineering)

Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
All Questions carry equal marks

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1. (a) What is instruction Cycle ?
   (b) Elaborate the characteristics of a hypothetical machine
   (c) What do you mean by hardwired program? [6+6+4]
2. Write an algorithm to substract binary numbers represented in normalized floating point mode with base 2 for exponent [16]
3. (a) Explain about cache management operation of power PC
   (b) List nine separate conditions for conditional branch instructions of power PC. [8+8]
4. (a) Discuss about RISC pipelining with regular instructions
   (b) How would you optimize RISC pipelining?
   (c) Give reasons for reduction in overall execution rate of RISC processors [8+4+4]
5. (a) Discuss about principles of cache memory.
   (b) Elaborate on elements of cache memory.
   (c) Explain the purpose of replacement algorithms [6+5+5]
6. Discuss three possible techniques for I/O operations with merits and demerits of each. [16]
7. (a) Explain about microinstruction format of TI 8800
   (b) Explain about ALU control fields of IBM 3033 microinstruction. [8+8]
8. (a) Differentiate between miltiprocessors and multicomputers.
   (b) Discuss about instruction pipeline. [7+9]

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