Code No: RR321503 **Set No. 1**

III B.Tech II Semester Regular Examinations, Apr/May 2006
FAULT TOLERANT SYSTEMS
(Computer Science & Systems Engineering)

Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
All Questions carry equal marks

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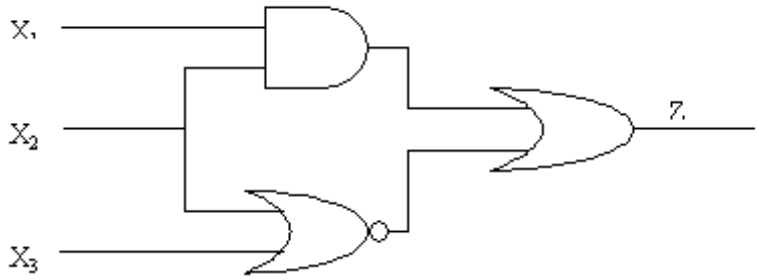
1. (a) Define the term Reliability of a system. Derive a relation for the R(t) in terms of constant failure rate λ. [3+5]
   (b) What is meant by Mean time between failures? How is it useful in system usage. Derive the expression of MTBF. [2+3+3]

2. (a) Illustrate the principles of path sensitizing method for the circuit given below and generate test vectors for different paths having different faults on them as shown in the figure1.



$Z = X_1X_2 + \overline{X}_2\overline{X}_3$

Figure 1:

   (b) How is path sensitization method advantageous over Fault Table method.Prove it for the above example. [8+8]

3. (a) Explain fail soft-operation. [4]
   (b) Explain the 5 MR reconfiguration mechanism and also explain how it care tolerate single, double and Trible faults in a given system. [3x4=12]

4. (a) What is the mechanism adopted in COPRA a fault Tolerant system. Explain in detail.
   (b) What is meant by Time redundancy? Explain. [4+4+4+4]

5. Build a self-testing checker for any
   (a) systematic error detecting codes.
   (b) systematic error detecting codes like Berger codes with I $=2^K$ - 1 data bits. [8+8]

6. (a) Explain the design consideration of self checking PLA considering stray faults with suitable example.
   (b) How do you implement strong fault service for the functional PLA. [8+8]

7. Explain the technique for designing minimally testable network which produces a circuit which can be tested by three tests only.Modify the function $f = \overline{A}\ \overline{B}$C +A $\overline{B}\ \overline{C}$ into a circuit which has only three tests. [10+6]

8. (a) What is meant by circular BIST technique?
   (b) Give a simplified configuration of circular BIST and explain. [8+8]

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Code No: RR321503 **Set No. 2**

III B.Tech II Semester Regular Examinations, Apr/May 2006
FAULT TOLERANT SYSTEMS
(Computer Science & Systems Engineering)

Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
All Questions carry equal marks

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1. (a) If a system has 4000 identical components with a failure rate of 0.02% per 1000 hours. Find the MTBF of such a system.
   (b) Explain the phenomenon of Bath tub response for a Time Vs failure rate of a system. [8+8]
2. (a) What are the goals of Design for testability?
   (b) Distinguish between ditermenistic test pattern generation and probabilitstic test pattern generation methods. [6+5+5]
3. (a) Explain different fault delection Techniques used in dynamic redundancy system. [3x3=9]
   (b) Draw a neat Hybrid (3,s) system and derive the R(t) of this system. Extend the derivation to Hybrid (N,S) system. [3+3+1]
4. Explain the scheme proposed by lala for incorporating redundancy in the design of digital systems on single chip. [4+4+4+4]
5. (a) Design a combinational self - testing checkers for k - out of 2 k codes, which are self-testing.
   (b) List out the importance and advantages of self - checking checker circuits. [8+8]
6. Design a sequential circuit using a partition theory for the given state table. [16]

	NS,	I/P,	Z	
PS	I_1	I_2	I_3	I_4
A	C,0	C,0	A,0	A,0
B	B,1	C,0	D,1	A,0
C	C,0	B,0	A,0	A,0
D	B,1	A,0	D,1	A,0
E	E,0	E,0	A,0	A,0

7. Explain the technique for designing minimally testable network which produces a circuit which can be tested by three tests only.Modify the function $f = \overline{A}\ \overline{B}$C +A $\overline{B}\ \overline{C}$ into a circuit which has only three tests. [10+6]
8. (a) What is meant by controllability? Explain with suitable examples. [3+5]
   (b) What is meant by Observability? Explain with suitable examples. [3+5]

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Code No: RR321503 **Set No. 3**

III B.Tech II Semester Regular Examinations, Apr/May 2006
FAULT TOLERANT SYSTEMS
(Computer Science & Systems Engineering)

Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
All Questions carry equal marks

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1. Derive the reliability function of a parallel ,series system compare the results with a fixed R(t) = 0.9 for each module used. [6+6+4]

2. (a) Illustrate the principles of path sensitizing method for the circuit given below and generate test vectors for different paths having different faults on them as shown in the figure1.

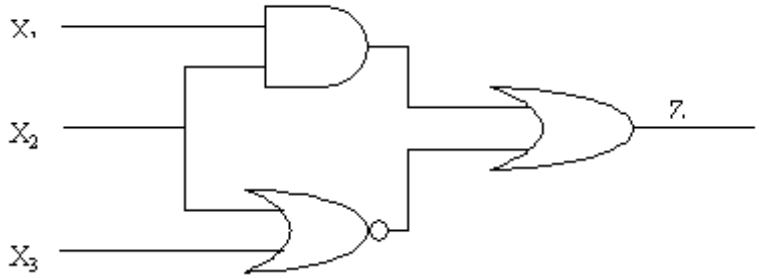

Figure 1:

(b) How is path sensitization method advantageous over Fault Table method.Prove it for the above example. [8+8]

3. (a) Construct a seven-bit error correcting code to represent the decimal digit by augmenting the Excess-3 code and by using add-1 parity check.

(b) Design a redundant circuit for $f = a \oplus b$ [9+7]

4. (a) With an example explain the practical fault tolerant system?

(b) How do you enhance the fault tolerance characteristics of digital systems.[8+8]

5. Build a self-testing checker for any

(a) systematic error detecting codes.

(b) systematic error detecting codes like Berger codes with I =2^K - 1 data bits. [8+8]

6. (a) Explain the design consideration of self checking PLA considering stray faults with suitable example.

(b) How do you implement strong fault service for the functional PLA. [8+8]

7. Write a short notes an [4x4=16]
   (a) Controllability
   (b) Observability
   (c) Positive unate function
   (d) Syndrom relations of all types of terminating gates.
8. Explain observability enhancement with neat diagram with suitable examples. [4+2+10]

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Code No: RR321503 **Set No. 4**

III B.Tech II Semester Regular Examinations, Apr/May 2006
FAULT TOLERANT SYSTEMS
(Computer Science & Systems Engineering)

Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
All Questions carry equal marks

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1. (a) Distinguish between failures, and faults. Explain. [2+2]
   (b) Explain the different modeling schemes of faults that generally come across in digital circuits. [3x2=6]
   (c) Explain the following terms with respect to digital circuits with suitable examples.
      i. Fault diagnosis.
      ii. Fault detection test set.
      iii. Test vector generation. [3x2=6]
2. Show that the 3 paths indicated in the circuit cannot be sensitized individually but can be sensitized simultaneously as show in figure1. [16]

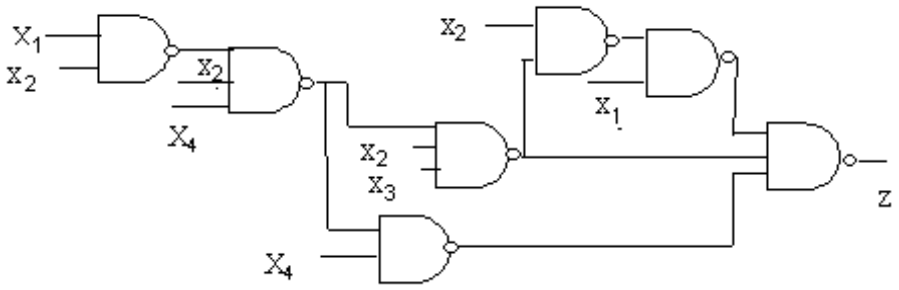

Figure 1:

3. (a) Find all the static hazards in the circuit shown in figure2 below (assume the individual elements to be hazard free).
   (b) Changing only the parameters of threshold element, redesign the circuit so that all static hazards are element are eliminated? [8+8]
4. (a) What is the goal of "pluibus" system used in ARPA network. Explain its working.
   (b) What is ment by fail soft operation? What should a system have to achieve the capability of fail soft operation. [4+4+4+4]
5. Build a self-testing checker for any
   (a) systematic error detecting codes.

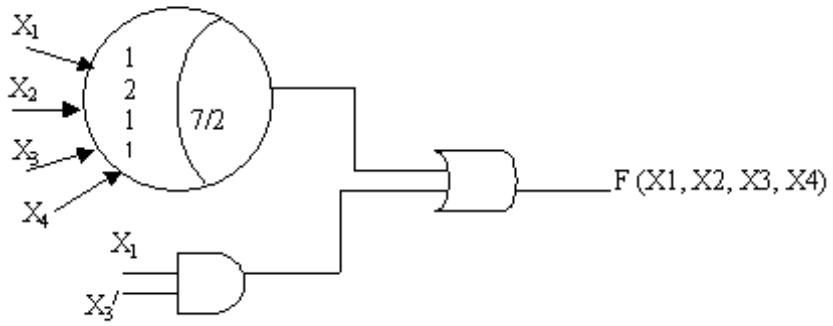

Figure 2:

(b) systematic error detecting codes like Berger codes with I $=2^K$ - 1 data bits. [8+8]

6. Explain in detail about fail-safe sequential circuits design with an example. [16]

7. (a) Explain the Reed-Muller expansion Technique used in Design for testable circuit.

   (b) Obtain the Reed Muller circuit for the given function. Also give the test set for the same.
   $f = AB + \overline{AC} + BC$ [8+4+4]

8. (a) Discuss the advantages of LSSD technique.

   (b) Discuss Random Access Scan Technique with example. [8+8]

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