

III B.Tech II Semester Regular Examinations, Apr/May 2006
ADVANCED COMPUTER ARCHITECTURE
(Common to Computer Science & Engineering, Information Technology
and Computer Science & Systems Engineering)

Time: 3 hours

Max Marks: 80

Answer any FIVE Questions
All Questions carry equal marks

1. Explain the fast computation applications in the following areas.
 - (a) Energy Resources exploration.
 - (b) Medical, Military and Basic Research. [8+8]
2. (a) What are the bottlenecks in pipeline processors? Suggest suitable methods to alleviate them.
(b) Describe the characteristics of vector processing. [8+8]
3. (a) Discuss the issues involved for Inter– PE Communication in array processors.
(b) What is a Multistage Network? Describe different types of multistage network. [8+8]
4. (a) Compare the two types of Associative Processor organizations.
(b) Differentiate between Bit-slice and Word-slice operations in STARAN. [10+6]
5. (a) With a block diagram explain the working of a unidirectional bus interconnection network for multiprocessor system. What are its advantages and drawbacks?
(b) Explain briefly the following bus arbitration algorithms and give their relative merits. [10+6]
 - i. The dynamic priority algorithm.
 - ii. The first-come first-served algorithm.
6. Briefly characterize the multicache coherence problem and describe various methods that can be used to cope with the problem. [16]
7. (a) Explain the organization of a static data flow computer.
(b) What are the major design issues of a data flow computer? Explain in detail. [8+8]
8. (a) Give architecture of the front-end system interface with Cray-1 memory and functions sections.
(b) Briefly explain the architecture of Cyber-205. [8+8]

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1. Explain different parallel processing mechanisms that are possible in uniprocessor computers. [16]
2. (a) Derive the expressions for efficiency, throughput and speed up for k stage pipeline for n tasks.
(b) What are key issues in the design of an efficient dynamic pipeline processor. [8+8]
3. (a) How are the two functions of a Shuffle Exchange are implemented?
(b) Compare the various Multistage SIMD Network. [10+6]
4. (a) Compare the two types of Associative Processor organizations.
(b) Differentiate between Bit-slice and Word-slice operations in STARAN. [10+6]
5. (a) List the several factors that affect the characteristics and performance of a bus.
(b) Explain the different Bus arbitration algorithms. [4+12]
6. (a) List the major characteristics, advantages and shortcomings of three types of multiprocessor operating systems.
(b) List the four main sources of performance degradation of the dynamic coherence check algorithm. [12+4]
7. (a) Differentiate between dependence driven and multi level event driven approach of designing data flow systems.
(b) Explain the functional design of a processor element in the EDDY system. [8+8]
8. (a) How memory mapping is done in Cyber-205? Explain
(b) List various functions of virtual memory in Cyber 205.
(c) Describe any two special vector instruction of Cyber 205. [8+8]

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1. (a) Explain the hierarchical memory system and how this concept is used to implement parallel processing.
 (b) What is Balancing of subsystem Band width? Explain how the different balancing techniques improve the parallelism? [8+8]
2. (a) What is the utility of a reservation table? Taking a suitable unifunction pipeline as an example, draw the reservation table and its state diagram.
 (b) What are reconfigurable pipelines? Explain the benefit of these pipelines with the help of a suitable example. [8+8]
3. (a) Explain the various configurations of an SIMD array Processors.
 (b) List down the similarities and differences between them. [10+6]
4. Describe a student – file search in a bit parallel associative memory- Assume relevant data. [16]
5. (a) Explain hierarchical structured multiprocessor system .
 (b) Describe processor characteristics for multiprocessing systems. [8+8]
6. (a) With the help of a diagram explain C-access memory organization. Is this memory organization be used for multiprocessors ? Explain.
 (b) Write a note on performance analysis of delta networks. [10+6]
7. (a) Compare Control flow computers against Data flow computers.
 (b) Explain with an example, how an instruction is executed in a data flow computer. [8+8]
8. (a) Explain the multitasking of crayX-MP for their following example.
 Do I = 2,N
 A(I) = A(I - 1) + B(I) S1
 D(I) = A(I) + C(I) S2
 Continue
 S1, S2 → stands for two vector computations.
 (b) Give the architecture of C.mmp multiprocessor system. [8+8]

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1. (a) What do you mean by parallel processing and what are the different levels at which parallel processing is achieved?
(b) Explain the concepts of Multiprogramming and time sharing, using these concepts explain how parallelism can be achieved in an uniprocessor system. [8+8]
2. (a) Differentiate between Static and Dynamic Pipelines.
(b) Compare and contrast Unifunctional and Multifunctional pipelines.
(c) Explain the concept of Instructional pipeline. [5+5+6]
3. Bring out the differences, merits and demerits of Rearrangeable, Non Blocking, and Blocking and Networks. Give an example commercial network for each one of them. [16]
4. Describe a student – file search in a bit parallel associative memory- Assume relevant data. [16]
5. (a) Explain briefly the communication between processors in a Multiprocessor environment.
(b) With suitable diagram, explain loosely coupled and tightly coupled Multiprocessors. [6+10]
6. (a) Explain briefly the requirements of software for multiprocessors .
(b) What is a master-slave operating system ? List its characteristics, advantages and shortcomings. [8+8]
7. (a) Describe data flow design alternatives.
(b) Explain the organization of the EDDY data flow machine. [8+8]
8. (a) How memory mapping is done in Cyber-205? Explain
(b) List various functions of virtual memory in Cyber 205.
(c) Describe any two special vector instruction of Cyber 205. [8+8]
