

III B.Tech II Semester Regular Examinations, Apr/May 2006
MICROPROCESSORS
 (Mechatronics)

Time: 3 hours

Max Marks: 80

Answer any FIVE Questions
 All Questions carry equal marks

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1. (a) Explain various interrupt pins of 8085 Microprocessor, and also write their priority.
 (b) What are the various status flags provided in 8085? Discuss their role. [8+8]
2. (a) Given that BX = 637D, SI = 2A9B, Displacement 237. Determine the effective resulting from these registers and the addressing made.
 - i. Immediate
 - ii. Direct
 - iii. Register Indirect using BX
 - iv. Relative Base Indexed
 - v. Base Indexed
 - vi. Register Relative using BX.
 (b) Explain the Flag register of 8086. Also show their positions in Flag register. [12+4]
3. (a) Explain the Fixed part and variable part formats of IN and OUT instructions with examples.
 (b) Write a program to check whether the given string is palindrome or not. [8+8]
4. (a) Write the sequence of statements that declare the word named 'NWORD' and FAR label 'EXTMOD' as being external and the variable 'IWORD' and the label 'LOCMOD' as being local and accessible by other source modules?
 (b) Give the sequence of instructions that pushes the offsets of word variables X, Y and Z in data segment onto stack? [8+8]
5. A logic network is having input variables A,B,C,D. The output variables are given

$$W = A.BC + ABC + AD$$

$$X = \underline{AC} + \underline{BA} + AD$$

$$Y = A.B + A.C + D.\underline{B}$$

$$Z = ABC + ACD + A.BC$$

The array INPUT-1 contains 10 different combinations of input variables. Write an instruction sequence that determine the outputs for each combination of INPUT-1 array and store the output variables in the string OUTPUT-1. [16]
6. Explain the following data transfer schemes.
 - (a) Programmed I/O

(b) Interrupted I/O

(c) DMA.

[5+5+6]

7. Explain how to interface a stepper motor with 4-step input sequence to 8086 based system with the help of hard ware design? Write the instruction sequence to move the stepper motor 10 steps in clockwise and 12 steps in anti-clockwise direction.

[16]

8. (a) What are the MODEM control lines? Explain the function of each line? Discuss how MODEM is controlled using these lines with necessary sequence of instructions?

(b) Discuss the Command instruction and Status register format of 8251? [8+8]

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1. (a) Explain the difference between Machine Language, Assembly Language and High Level language.
(b) Explain the requirement of a program counter, stack pointer and status flags in the architecture of Intel 8085 Micro process. [8+8]
2. (a) Explain the Execution unit of 8086.
(b) Explain about memory segmentation and Queue. [8+8]
3. (a) Write a program to move a block of memory with out over lapping.
(b) Write about the following instructions.
 - i. ADC
 - ii. AAS
 - iii. IMUL
 - iv. CBW[8+8]
4. A set of code is reused several times with a separate stack in a program. The reminder of the program uses another stack segment. Define a macro with the necessary instructions at the beginning and end of this set of code in order to switch stacks and then switch back again. Also give the necessary code to define the two stacks and initially set SS and SP? [16]
5. (a) It is necessary to move a block of data of length 200H from location 4000H:A000H to location 0B000H:B000H. Write an instruction sequence using string instructions?
(b) Discuss the hierarchical design for a simple text editor? [8+8]
6. (a) What are the different control signals necessary for I/O read and write cycles? Show how these control signals are generated in minimum and maximum modes of 8086?
(b) Design an I/O port decoder that generate the following low-bank I/O strobes: 00FEH, 00C8H, 00DEH, 00EEH? [8+8]
7. Interface a 12-bit DAC to 8255 with an address map of 0C00H to 0C03H. The DAC provides output in the range of +5V to -5V. Write the instruction sequence.
 - (a) For generating a square wave with a peak to peak voltage of 4V and the frequency will be selected from memory location 'F'.

- (b) For generating a triangular wave with a maximum voltage of $+3V$ and a minimum of $-2V$. [8+8]
8. (a) What is the difference between 20mA current loop and RS232-C standard?
- (b) Explain the necessity of RS232 to TTL interface and draw the circuit?
- (c) Draw the circuit of TTL to RS232 and explain the necessity of this interface. [5+5+6]

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1. (a) Explain various interrupt of 8085 Microprocessor and their priorities.
(b) Explain the
 - i. SID
 - ii. SOD
 - iii. S_0, S_1 ,
 - iv. \overline{INTA} pins of 8085 Microprocessor[8+8]
2. (a) Explain the flag register of 8086.
(b) Explain the concept of memory segmentation.
(c) Explain, when Queue is failing to speed up the execution. [6+6+4]
3. (a) Explain the following Instructions.
 - i. MOV
 - ii. POP
 - iii. XCHG
 - iv. SAHF
(b) Write a program to convert a Binary Number to a BCD Number. [8+8]
4. A set of code is reused several times with a separate stack in a program. The remainder of the program uses another stack segment. Define a macro with the necessary instructions at the beginning and end of this set of code in order to switch stacks and then switch back again. Also give the necessary code to define the two stacks and initially set SS and SP? [16]
5. (a) Explain string instructions supported by 8086 processor?
(b) Give the instruction sequence that compares the first 10 bytes beginning at STRG_1 with the first ten bytes beginning at STRG_2 and branches to MATCH if they are equal, otherwise continues in sequence? [8+8]
6. (a) What is the minimum no. of bus cycles that can occur between the time an interrupt request is recognized and the first instruction in the interrupt service routine is fetched. Show the interrupt acknowledge cycle with a flow chart?
(b) Show the complete hardware design to resolve multiple interrupts based on priority using Daisy chain? [8+8]
7. (a) What is BSR mode operation? How it is useful in controlling the interrupt initiated data transfer for mode 1 and 2?

- (b) Explain the transistor buffer circuit used to drive 7-segment LEDs? [8+8]
8. (a) Draw the command register and mode register format of 8237 and explain each bit?
- (b) Show how 8237s are cascaded to provide more number of DRQs and explain the operation?
- (c) Explain how memory to memory transfer is performed with 8237? [6+5+5]

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1. (a) Explain various interrupt pins of 8085 Microprocessor, and also write their priority.
(b) What are the various status flags provided in 8085? Discuss their role. [8+8]
2. (a) Explain the different types of Instruction Formats used in 8086
(b) Give the sum and Flag settings for AF, SF, ZF, CF, OF, and PF after hexadecimally adding 62A0 to each of the Following:
 - i. 1234
 - ii. 9090
 - iii. 9060[10+6]
3. (a) Explain the following Instructions.
 - i. MOV
 - ii. POP
 - iii. XCHG
 - iv. SAHF(b) Write a program to sort an array in descending order [8+8]
4. (a) Discuss the difference between intra segment and inter segment procedures? Explain the return procedure in the above cases? Give the sequence of statements for defining the above procedures and return methods?
(b) Give the necessary statements to permit the byte variables NUM1, NUM2, NUM3 and NUM4 which are defined in source module 2 to be accessed in source module 1 as if they are defined in source module 1? [8+8]
5. (a) Write an assembly language program that will examine an ASCII string of 100 characters and replace each decimal digit by a %. The character string starts at STRG. [7]
(b) Explain the following instructions and their use?
 - i. LODSB
 - ii. CMPSW
 - iii. XLAT[3+3+3]
6. (a) Give the instruction format of IN and OUT instructions and explain?
(b) Draw a flow chart showing how a block of N bytes are inputted to memory using programmed I/O transfer? [8+8]

7. It is necessary to initialize interrupt for mode 2 operation of port-A and mode 1 operation of port-B with the 8255 address map of 0800H to 0803H. Give the complete hardware design to interface 8255 to 8086 processor with this address map? Write the instruction sequence for the initialization of 8255 in the above modes? Give the instruction sequence to change the operation modes of port A and Port B to mode 1? [16]
8. (a) Explain demand transfer mode and block transfer mode of 8237?
(b) Show how 8237s are cascaded to provide more number of DRQ's and explain the operation?
(c) Explain how memory to memory transfer is performed with 8237? [6+5+5]
