Code No: RR420203 **Set No. 1**

IV B.Tech II Semester Regular Examinations, Apr/May 2006
VLSI DESIGN
(Electrical & Electronic Engineering)

Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
All Questions carry equal marks

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1. (a) With neat sketches explain the drain characteristics of an n-channel enhancement MOSFET.
   (b) n-MOS Transistor is operated in the Active region with the following parameters $V_{GS} = 3.9V$; $V_{tn} = 1V$; $W/L = 100$; $\mu nCox = 90\ \mu A/V^2$
   Find its drain current and drain source resistance. [8+8]
2. With neat sketches explain how Diodes and Resistors are fabricated in Bipolar process. [16]
3. Design a stick diagram for the CMOS logic shown below $Y = \overline{(A + B + C)}$ [16]
4. Design a layout diagram for the CMOS logic shown below $Y = \overline{(A + B).C}$ [16]
5. Calculate ON resistance from V_{DD} to GND for the given inverter circuit shown in Figure 1, If n-channel sheet resistance is $10^4\Omega$ per square. [16]

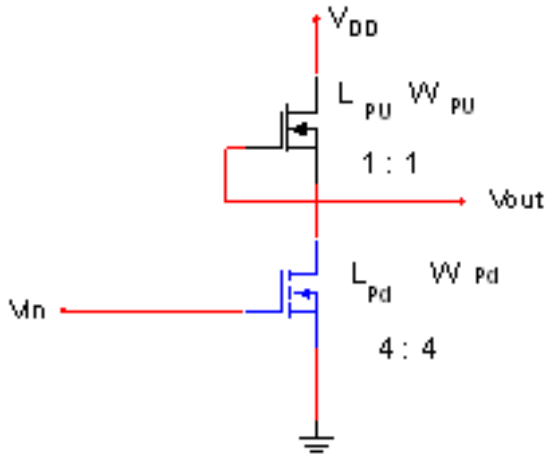

Figure 1:

6. Using PLA Implement JK Flip flop circuit. [16]
7. What are the inputs that are provided to the synthesis tool? And explain completely about synthesis process in the ASIC design. [16]
8. Mention different growth technologies of the thin oxides and explain about any one technique. [16]

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Code No: RR420203 **Set No. 2**

IV B.Tech II Semester Regular Examinations, Apr/May 2006
VLSI DESIGN
(Electrical & Electronic Engineering)

Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
All Questions carry equal marks

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1. (a) Clearly explain the body effect of the MOSFET.
   (b) Clearly explain about channel length modulation of the MOSFET. [8+8]
2. (a) Compare between CMOS and bipolar technologies.
   (b) With neat sketches explain nMOS fabrication process. [8+8]
3. Design a stick diagram for the CMOS logic shown below $Y = \overline{(A+B).C}$ [16]
4. Design a layout diagram for two input CMOS NOR gate. [16]
5. Calculate on resistance of the circuit shown in Figure 1 from V_{DD} to GND. If n-channel sheet resistance Rsn = 10^{4} Ω per square and p-channel sheet resistance $Rsp = 4.5 \times 10^{4}\Omega$ per square. [16]

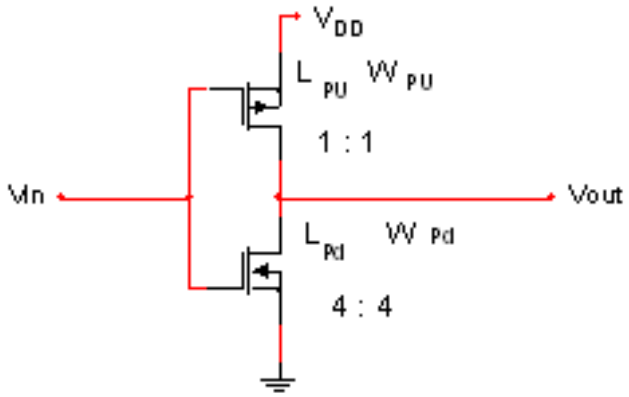

Figure 1:

6. Implement 4-2 Encoder using PROM. [16]
7. (a) What is the goal of VHDL synthesis step in design flow?
   (b) Explain how register transfer level description provides optimized synthesis netlist. [8+8]
8. Clearly explain the wire bonding technology of the die bonding. [16]

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Code No: RR420203 **Set No. 3**

IV B.Tech II Semester Regular Examinations, Apr/May 2006
VLSI DESIGN
(Electrical & Electronic Engineering)

Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
All Questions carry equal marks

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1. (a) Derive an equation for I_{DS} of an n-channel Enhancement MOSFET operating in linear region.
   (b) A PMOS transistor is operating in saturation region with the following parameters. $V_{GS} = -5V$; $V_{tp} = -1.2V$; $W/L = 95$; $\mu nCox = 95\ \mu A/V^2$ Find Trans conductance of the device. [8+8]
2. With neat sketches explain BICMOS fabrication in an n-well process. [16]
3. Design a stick diagram for the PMOS logic shown below $Y = \overline{(AB + CD)}$ [16]
4. Design a layout diagram for nMOS inverter. [16]
5. Derive an equation for the propagation delay from input to output of the pass transistor chain shown in Figure 1. [16]

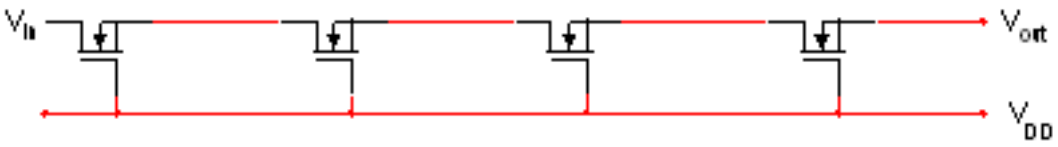

Figure 1:

6. Implement 4-2 Encoder using PROM. [16]
7. (a) Define the term DFT and explain about it.
   (b) Explain any one test procedure to test sequential logic. [8+8]
8. Mention different growth technologies of the thin oxides and explain about any one technique. [16]

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Code No: RR420203 **Set No. 4**

IV B.Tech II Semester Regular Examinations, Apr/May 2006
VLSI DESIGN
(Electrical & Electronic Engineering)

Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
All Questions carry equal marks

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1. (a) Derive an equation for I_{DS} of an n-channel Enhancement MOSFET operating in Saturation region.
   (b) An nMOS transistor is operating in saturation region with the following parameters. $V_{GS} = 5V$; $V_{tn} = 1.2V$; $W/L = 110$; $\mu nCox = 110\ \mu A/V^2$. Find Transconductance of the device. [8+8]

2. (a) With neat sketches explain CMOS fabrication using n-well process.
   (b) Explain how capacitors are fabricated in CMOS process. [10+6]

3. Design a stick diagram for the CMOS logic shown below $Y = \overline{(A + B + C)}$ [16]

4. Design a layout diagram for the PMOS logic shown below $Y = \overline{(AB) + (CD)}$ [16]

5. Calculate ON resistance from V_{DD} to GND for the given inverter circuit shown in Figure 1, If n-channel sheet resistance is $10^4\Omega$ per square. [16]

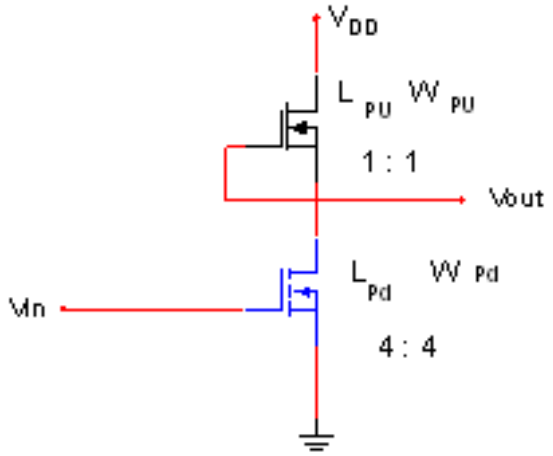

Figure 1:

6. (a) What are the advantages and disadvantages of the reconfiguration.
   (b) Mention different advantages of Anti fuse Technology. [8+8]

7. Clearly explain each step of high level design flow of an ASIC. [16]

8. With neat sketches explain the oxidation process in the IC fabrication process. [16]

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