II B.Tech. I Semester Supplementary Examinations, May -2005
SWITCHING THEORY AND LOGIC DESIGN
(Common to Electrical & Electronic Engineering, Electronics & Communication Engineering, Computer Science & Engineering, Electronics & Instrumentation Engineering, Bio-Medical Engineering, Information Technology, Electronics & Control Engineering, Computer Science & Systems Engineering, Electronics & Telematics and Electronics & Computer Engineering)

Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
All Questions carry equal marks

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1. (a) Perform the subtraction with the following unsigned binary numbers by taking the 2's complement of the subtrahend.
   i. 11010-10000
   ii. 11010-1101
   iii. 100-110000
   iv. 1010100-1010100
   (b) The binary numbers listed have a sign bit in the left most position and, if negative, are in 1's complement form. Perform the arithmetic operations indicated and verify the answers.
   i. 101011+111000
   ii. 001110+110010
   iii. 111001-001010
   iv. 101011-100110

2. (a) Minimize the function using Karnaugh-Map and obtain minimal sop function. f(A,B,C,D) = π (1,2,3,8,9,10,11,14) +$\sum$d (7,15).
   (b) Determine canonical POS form for the function T $(x, y, z) = x(\overline{y} + z)$.
   (c) Prove that Y=AB + BC + AC is a self dual function.

3. Using the Quine-Mc Cluskey method of tabular reduction ,minimize the given combinational single - output function f(w,x,y,z) = $\sum$m(0,1,5,7,810,14,15)

4. (a) Design a full-adder with two half-adders and basic gates.
   (b) Convert Excess-3 code to BCD using Full adder circuits.

5. (a) Define the following terms in connection with a Flip-Flop
   i. set-up time
   ii. hold time
   iii. propagation delay-time

(b) For the block diagram shown , draw the schematic circuit using NAND gates & explain its operation with the help of truth table.

6. (a) Compare merits and demerits of ripple and synchronous counters.

   (b) Design a modulo-12 up synchronous counter using T-flip flops and draw the circuit diagram.

7. Obtain equivalent classes using partition method and give proper assignment.

PS	NS,Z	
	X-0	X=1
A	F,0	B,0
B	D,0	C,0
C	F,0	E,0
D	G,1	A,0
E	D,0	C,0
F	F,1	B,1
G	G,0	H,1
H	G,1	A,0

8. Design a half adder and half subtractor circuit using

   (a) multiplexer and registers

   (b) one flipflop per state..Draw the state diagram and convert it to ASM block and tablulate its state table.

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   i. 101011+111000
   ii. 001110+110010
   iii. 111001-001010
   iv. 101011-100110

2. (a) i. Find the complement of the Boolean function (B$\overline{C}$+ $\overline{A}$D)(A$\overline{B}$+C$\overline{D}$)and reduce it to a minimum number of literals.
   ii. Convert the function f(x,y,z) = π(0,3,6,7) to the other canonical form.
   (b) Simplify the Boolean function F in sum of products using the don't care conditions d: (Karnaugh map method)
   F=$\overline{y} + \overline{xz}$
   $d = yz + xy$

3. (a) Implement the following Boolen function F together with the dont care conditions D using not more than two NOR gates. Assume that both normal and complement inputs are available.
   $F(A, B, C, D) = \sum$(0.1.2.9,11)
   $D(A, B, C, D) = \sum$ (8,10,14,15)
   (b) What are universal gates. Why they are so called. Give their truth tables.

4. (a) Give the implementation of a 4-bit ripple-carry adder using half- adder(s) / full-adder(s).

(b) Explain with an example , the mux and demux can be used as data - selector and data-distributor respectively.

5. (a) Define the following systems
   i. synchronous sequential system
   ii. asynchronous sequential system
   iii. combinational system

   (b) Draw the schematic circuit of a negative edge triggered D-Flip-Flop using NAND gates and give its truth-table. Justify the entries in the truth-table.

6. (a) Draw the state diagram for the synchronous sequential circuit with inputs (x_1, x_2) and single output z in which the input pair represents alphabet letters as given below.
   A-00
   B-01
   C-10
   D-11
   The output is 1 if the most recent two inputs are in alphabetic order (i.e.) AB, BC and CD.

   (b) Draw the circuit diagram of R-S flip flop with active low preset and clear with level mode clock. What is the disadvantage in using level mode clock? How to overcome this problem. Discuss.

7. (a) Distinguish between Mealy and Moore machines

   (b) Convert the following Mealy machine into a corresponding Moore machine:

PS	NS,Z	
	X-0	X=1
A	B,0	E,0
B	E,0	D,0
C	D,1	A,0
D	C,1	E,0
E	B,0	D,0

8. (a) Draw the state diagram and the state table of the control unit conditions given below. Draw the equivalent ASM chart leaving the state box empty.
   i. from 00 state, if x = 1 , it goes to 01 state and if x = 0, it remains in the same state 00.
   ii. from 01 state, if y = 1, it goes to 11 state and if y = 0, it goes to 10 state.
   iii. from 10 stae, if x = 1 and y = 0, it remains in the same state 10 and if x = 1 and y = 1, it goes to 11 state, and if x = 0, it goes to 00 state.
   iv. from 11 state, if x = 1, y = 0, it goes to 10 state and if x = 1, and y = 1, it remains in the same state, and if x = 0, it goes to 00 state.

   (b) Design the control with multiplexers for the above problem

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Code No: RR210203 **Set No.3**

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Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
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1. (a) i. Express decimal digits 0-9 in BCD code and 2-4-2-1 code.
   ii. Determine which of the above codes are self complementing.
   (b) i. Convert the decimal number 96 into binary and convert it to gray code number.
   ii. Convert the given gray code number to binary: 1001001011.

2. For the given function
   $$F(A, B, C, D) = \sum (0,1, 2, 3, 4, 5, 9, 10, 16, 17, 18, 19, 20, 22, 25, 26) + \sum d\ (7, 11, 12, 13, 15, 23, 27, 28, 29, 30)$$
   Obtain minimal sop expression using K-Map.

3. (a) Derive Boolean expression for a 2input Ex-OR gate to realize with 2 input NAND gates without using complemented variables and draw the circuit.
   (b) Redraw the given circuit in (figure1)after simplification .

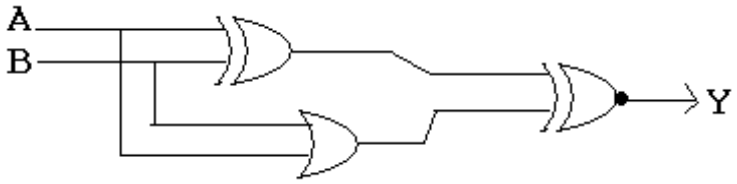

Figure 1:

4. (a) Design 64 line output demultiplexer using lower order demultiplexer. Such as 4 to 16 and 2 to 4 Demultiplexers.
   (b) Give the NAND gate realization of full-adder.

5. (a) Define a sequential system and how does it differ from a combinational system
   (b) Augment an S-R Flip-Flop with two AND gates to form a J-K-Flip-Flop and explain its operations with the help of Truth-Table

6. Design a modulo 6 up/down synchronous counter using T flip flops and draw the circuit diagram.

7. (a) Convert the following Mealy machine into a corresponding Moore machine:

PS	NS,Z	
	X=0	X=1
A	C,0	B,0
B	A,1	D,0
C	B,1	A,1
D	D,1	C,0

   (b) Design the circuit for the above table.

8. (a) Design a digital system with three 4-bit registers, A, B and C to perform the following operations by drawing the ASM chart.
      i. Transfer two binary numbers to A and B when a start signal is enabled.
      ii. If A<B, shift left the contents of A and transfer the result to register C.
      iii. If A>B, shift right the contents of B and transfer the result to register C.
      iv. If A+B, transfer the number to register C unchanged.

   (b) Realize the above using JK flipflops and D flip flops.

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1. (a) Give the Gray-code equivalent of the Hex number 3A7.
   (b) Find the Gray-code equivalent of the octal number 527.
   (c) When a block of data is stored on magnetic tape, some times parity is computed on both the rows and columns. Create the row and column parity bits for the data group shown below using odd parity.
   DATA
   10110
   10001
   10101
   00010
   11000
   00000
   11010
   (d) Obtain the 3 bit and 4 bit Gray codes from the 2 bit Gray code by reflection.

2. Four persons, members of a TV panel game, each have an ON/OFF button that is used to record their opinion of a certain pop record. Instead of recording individual scores, some data processing is required such that the score board shows a HIT when the majority vote is in favour of and a MISS if it is against Provision must also be made for a TIE. From this verbal statement.
   (a) Derive the truth tables separately for HIT, MISS and TIE.
   (b) Extract S-O-P and P-O-S for each of the three outputs.
   (c) Simplify the equation in SOP form.

3. Using the Quine-Mc Cluskey method of tabular reduction ,minimize the given combinational single - output function f(w,x,y,z) = $\sum$m(0,1,5,7,810,14,15)

4. (a) Design a combinational circuit that accepts a 3-bit number and generates an output binary number equal to the square of the input number.
   (b) Realize a 3-bit odd-parity generator circuit using only two-input ex-or gate

5. (a) Distinguish between combinational logic and sequential logic
   (b) Draw the schematic circuit of an edge triggered J-K - Flip-Flop with "active low preset" and "active low clear" using NAND gates and explain its operations with the help of Truth-Table.

6. A counter is to be designed to count either in 5421 code or 8421 code based on a control signal input. Draw the state diagram for such a counter and synthesize it using T flip flops. Assume that the control signal cannot change in the middle of a counting sequence.

7. For the machine shown in the table below obtain:
   (a) The corresponding reduced machine table in standard form
   (b) Find a minimum length that distinguishes state A from state B where PS: present state, NS: next state, Z: output, X: input

PS	NS,Z	
	X=0	X=1
A	B,1	H,1
B	F,1	D,1
C	D,0	E,1
D	C,0	F,1
E	D,1	C,1
F	C,1	C,1
G	C,1	D,1
H	C,0	A,1

8. Construct an ASM block that has 3 input variables (A,B,C), 4 output (W,X,Y,Z) and 2 exit paths. For this block, output Z is always 1, and W is 1 if A & B are both 1. If C=1 & A=0, Y=1 and exit path 1 is taken. If C=0 or A=1, X=1 and exit path 2 is taken.
   Realize the above using the One flip flop per state.

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