Code No: NR210203 **NR**

II B.Tech I Semester Supplementary Examinations, May 2005
SWITCHING THEORY & LOGIC DESIGN
(Common to Electrical & Electronic Engineering, Electronics & Communication Engineering, Computer Science & Engineering, Electronics & Instrumentation Engineering, Information Technology, Electronics & Control Engineering, Computer Science & Systems Engineering, Electronics & Telematics and Electronics & Computer Engineering)

Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
All Questions carry equal marks

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1. (a) Perform the subtraction with the following unsigned binary numbers by taking the 2's complement of the subtrahend.
   i. 11010-10000
   ii. 11010-1101
   iii. 100-110000
   iv. 1010100-1010100
   (b) The binary numbers listed have a sign bit in the left most position and, if negative, are in 1's complement form. Perform the arithmetic operations indicated and verify the answers.
   i. 101011+111000
   ii. 001110+110010
   iii. 111001-001010
   iv. 101011-100110

2. (a) i. Given $\overline{AB} + \overline{A}B = C$, Show that $\overline{AC} + \overline{A}C = B$.
   ii. $(A + B)(\overline{A} + C)(\overline{B} + D)(+C\overline{D})$;simplify
   (b) Define the connective * for the two valued variables A, B, and C as follows
   $A * B = AB + \overline{A}\ \overline{B}$
   Let C = A*B, Determine which of the following is valid
   i. A=B*C
   ii. B=A*C
   iii. A*B*C=1

3. Use the tabulation procedure to generate the set of prime implicants and to obtain all the minimal expressions for the following function
   G(w,x,y,z)=$\sum$m(0,1,4,5,6,7,9,11,15) +$\sum$d(10,14)

4. Implement the following functions using
   (a) PLA
   (b) PAL

$F_1(a,b,c,d) = \sum m(0,1,2,3,6,9,11)$
$F_2(a,b,c,d) = \sum m(0,1,6,8,9)$

5. (a) Define the following terms in connection with a flip-flop
   i. set-up time
   ii. hold-time
   iii. propagation delay time
   iv. preset
   v. clear

   (b) Draw the schematic circuit of D-Flip-Flop with negative edge triggering using NAND gates. Give its truth-table and explain its operation

6. (a) Draw the state diagram for the synchronous sequential circuit with inputs (x_1, x_2) and single output z in which the input pair represents alphabet letters as given below.
   A-00
   B-01
   C-10
   D-11
   The output is 1 if the most recent two inputs are in alphabetic order (i.e.) AB, BC and CD.

   (b) Draw the circuit diagram of R-S flip flop with active low preset and clear with level mode clock. What is the disadvantage in using level mode clock? How to overcome this problem. Discuss.

7. (a) Distinguish between Mealy and Moore machines

   (b) Convert the following Mealy machine into a corresponding Moore machine:

PS	NS,Z	
	X-0	X=1
A	B,0	E,0
B	E,0	D,0
C	D,1	A,0
D	C,1	E,0
E	B,0	D,0

8. (a) Draw the state diagram and the state table of the control unit conditions given below. Draw the equivalent ASM chart leaving the state box empty.
   i. from 00 state, if x = 1 , it goes to 01 state and if x = 0, it remains in the same state 00.
   ii. from 01 state, if y = 1, it goes to 11 state and if y = 0, it goes to 10 state.
   iii. from 10 stae, if x = 1 and y = 0, it remains in the same state 10 and if x = 1 and y = 1, it goes to 11 state, and if x = 0, it goes to 00 state.
   iv. from 11 state, if x = 1, y = 0, it goes to 10 state and if x = 1, and y = 1, it remains in the same state, and if x = 0, it goes to 00 state.

(b) Design the control with multiplexers for the above problem

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