

II B.Tech I Semester Supplementary Examinations, May 2005
PULSE & DIGITAL CIRCUITS
 (Common to Electrical & Electronic Engineering, Electronics &
 Communication Engineering, Electronics & Telematics and Electronics &
 Computer Engineering)

Time: 3 hours

Max Marks: 80

Answer any FIVE Questions
All Questions carry equal marks

1. (a) The periodic ramp voltage shown is applied to a low pass RC circuit. Find the equations from which to determine the steady state output waveform. (figure1)

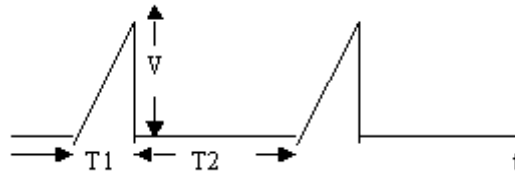


Figure 1:

- (b) If $T_1 = T_2 = RC$, find the maximum and minimum value of the output voltage and plot this waveform.
2. (a) What is synchronized clamping? Explain.
 (b) Design a diode clamper circuit to clamp the positive peaks of the input signal at zero level. The frequency of the input signal is 500 Hz.
3. (a) Explain the phenomenon of “latching” in a transistor switch.
 (b) A transistor has $f_T = 50$ MHz, $4_{FE} = 40$, $C_{b'c} = 3$ PF and operates with $V_{cc} = 12$ V and $R_c = 500 \Omega$. The transistor is operating initially in the neighbourhood of the cut-in point. What base current must be applied to drive the transistor to saturation in 1μ sec?
4. Explain how to draw the various waveforms and calculate their voltage levels in an emitter-coupled monostable multi.
5. With reference to voltage sweeps explain the following terms:
- Sweep speed
 - Linearity of sweep
 - Sweep stability
 - Recovery time.
6. (a) Explain how a sinusoidal oscillator can be used as a frequency divider.

- (b) Write short notes on
 - i. Phase delay and
 - ii. Phase jitters
- 7. (a) Differentiate a sampling gate from logic gate with an example?
(b) Discuss about sampling gates in detail.
- 8. What is meant by blocking oscillator? Explain the principle of a operation monostable blocking oscillator with base timing. Sketch the current waveforms and derive an expression for current pulse width.

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