Code No: RR222201 **Set No.1**

II B.Tech. II Semester Regular Examinations, April/May -2005
SWITCHING THEORY AND LOGIC DESIGN
(Instrumentation & Control Engineering)

Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
All Questions carry equal marks

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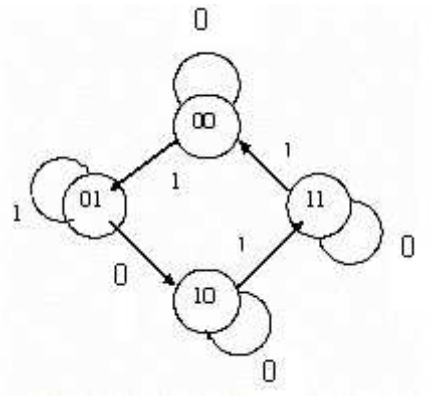
1. Convert the following numbers
   (a) $(1432)_8$ to base 10
   (b) 10101100111.0101 to base 10
   (c) 11010011001.1010 to base 8 and base 4
   (d) $(2002)_{10}$ to base 8
   (e) $(2002)_{10}$ to base 6
   (f) $(75.125)_{10}$ to base 2
   (g) $(3.375)_{10}$ to base 8 and base 2
   (h) $(ABCD)_{16}$ to base 10

2. (a) Obtain the simplified expressions in sum of products for the following Boolean functions using Karnaugh-Map.
      i. F(A, B,C,D) = Σ (7,13, 14, 15)
      ii. F(w,x,y,z) = Σ (2,3,12,13,14,15)
   (b) Minimize the following Boolean expressions to the required no. of literals
      i. BC + A$\overline{C}$+AB + BCDtofourliterals
      ii. ABC+$\overline{AB}$C+$\overline{A}$BC + AB$\overline{C}$+$\overline{ABC}$tofiveliterals*and*
   (c) Obtain complement and dual for the given expression (AB+BC+AC) (EF).

3. (a) Implement the following function using only NOR gates
   F = a.(b + c.d) + (b.$\overline{c}$).
   (b) Implement the following function using only NAND gates
   G = (a+$\overline{b}$).(c.d+$\overline{e}$)
   (c) Give the minimum two-level SOP realization of the following switching function using only NAND gates. F(x,y,z) = Σ m (0,3,4,5,7).

4. (a) Design a full-adder with two half-adders and basic gates.
   (b) Convert Excess-3 code to BCD using Full adder circuits.

5. (a) Define a sequential system and how does it differ from a combinational system?
   (b) Draw the schematic circuit of a negative edge-trigger S-R-Flip-Flop with "active low preset" and "active low clear" inputs using NAND gates and explain its operation with the help of Truth-Table.



6. Design the sequential circuit specified by the state diagram using T flipflops.

7. For the machine given below, find the equivalence partition and a corresponding reduced machine in standard form:

PS	NS, Z	
	X=0	X=1
A	D, 0	H, 1
B	F, 1	C, 1
C	D, 0	F, 1
D	C, 0	E, 1
E	C, 1	D, 1
F	D, 1	D, 1
G	D, 1	C, 1
H	B, 1	A, 1

8. Construct an ASM block that has 3 input variables (A,B,C), 4 output (W,X,Y,Z) and 2 exit paths. For this block, output Z is always 1, and W is 1 if A and B are both 1. If C=1 and A=0, Y=1 and exit path 1 is taken. If C=0 or A=1, X=1 and exit path 2 is taken.
   Realize the above using the PLA control and give the PLA table.

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Code No: RR222201 **Set No.2**

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Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
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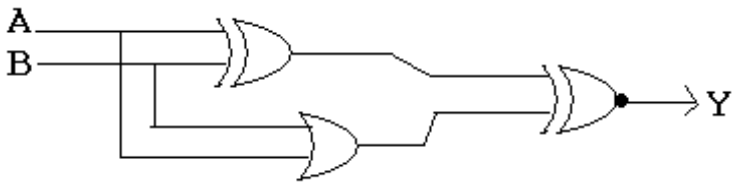
1. (a) Convert the following numbers to be indicated basses.
   i. 7562.45 to octal
   ii. 1938.257 to hexadecimal
   (b) Add and multiply the following numbers without converting to decimal
   i. $(367)_8$ and $(715)_8$
   ii. $(15F)_{16}$ and $(A7)_{16}$
   (c) Add in BCD form (98) and (87).

2. (a) Obtain the simplified expression in sum of products for the following Boolean functions using Karnaugh-Map.
   i. F(w, x, y, z) =$\Sigma(1, 3, 7, 11, 15)+\Sigma_d(0, 2, 5)$
   ii. F(A, B, C, D)*and*= ABD+$\overline{A}CD + \overline{A}B + \overline{A}C\overline{D} + A\overline{B}D$
   (b) Show the truth table for each of the following function and find its simplest product of sums form.(POS)
   i. f(x,y,z) = xy+xz
   ii. f(x, y, z) =$\overline{x}$+y$\overline{z}$.

3. (a) Derive Boolean expression for a 2input Ex-OR gate to realize with 2 input NAND gates without using complemented variables and draw the circuit.
   (b) Redraw the given circuit after simplification.



4. (a) Give the schematic circuit for a BCD-to-decimal decoder. Give the truth-table for the same.
   (b) A combinational circuit is specified by the following two Boolean functions Design the circuit with a decoder and basic gates.
   F =Σ m (1,5,9,15)
   G = Σ m (0,1,9,10,12).

5. (a) Define a combinational system and a sequential system and how does they differ from each other

   (b) Draw the schematic circuit of "Master-slave J-K-Flip-Flop" using NAND gates and explain its operation with the help of Truth-Table.

6. Design a sequential circuit with two D flipflops A and B and one input x. When x=0, the state of the circuit remains the same. When x=1, the circuit goes through the state transitions from 00 to 01 to 11 to 10 back to 00 and repeats.

7. (a) Convert the following Mealy machine into a corresponding Moore machine:

PS	NS, Z	
	X=0	X=1
A	C, 0	B, 0
B	A, 1	D, 0
C	B, 1	A, 1
D	D, 1	C, 0

   (b) Design the circuit for the above table.

8. Construct an ASM block that has 3 input variables (D,E,F) and 4 output variables (P,Q,R,S) and 2 exit paths. For this block, output P is always 1, and Q is 1 if D=1. If D and F are 1 or if D and E are 0, R=1 and exit path 2 is taken. If (D=0 and E=1) or (D=1 and F=0), S=1 and exit path 1 is taken. Realize it with multiplexer and register.

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Code No: RR222201 **Set No.3**

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Time: 3 hours **Max Marks: 80**

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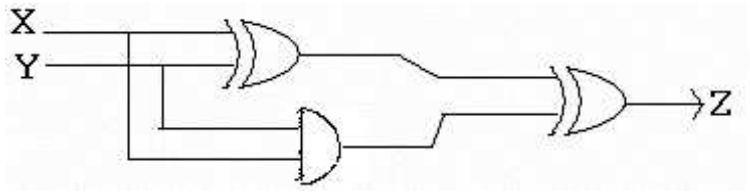
1. (a) Given the numbers a=1010.1, b=101.01, c=1001.1 perform the following binary operations
   i. a+c
   ii. (a-b) in 2's complement form
   (b) Find the 1's and 2's complements of the following 8-digit binary numbers
   i. 10101110
   ii. 10000001
   iii. 10000000
   iv. 00000000.

2. (a) Minimize the function using Karnaugh map method f (A,B,C,D) = Σm (1,3,5,8,9,11) + Σd (2,13).
   (b) Simply the given expressions using Boolean theorem
   i. f = AB + A$\overline{C}$+C + AD + A$\overline{B}$C + ABC.
   ii. $(\overline{x} + xy\overline{z}) + (\overline{x} + xy\overline{z})\,(x + \overline{xy}z)$
   iii. $a + \overline{a}b + \overline{a}\,\overline{b}c + \overline{a}\,\overline{b}\,\overline{c}d$+.....

3. (a) Derive Boolean expression for a 2 input Ex-NOR gate to realize with two input NOR gates, without using complemented variables and draw the circuit.
   (b) Redraw the given circuit after simplification.



4. (a) Show how a 16-to-1 mux can be realized using 4-to-1 muxes.
   (b) Implementthefunctionf(a, b, c) = a.b+$\overline{b}$.cusingthe4 − to − 1mux.

5. (a) Define a latch. Draw the schematic circuit of D-Latch using NAND gates and explain its operations.
   (b) Draw the schematic circuit of J-K Master-slove Flip-Flop with active low clear and preset inputs and explain its operation with the help of Truth-Table

6. Design a sequential circuit with two JK flipflops A and B and two inputs E and x. If E=0, the circuit remains the same state regardless of the value of x. When E=1 and x=1, the circuit goes through the state transition from 00 to 01 to 10 to 11 back to 00 and repeats. When E=1 and x=0, the circuit goes through the state transitions from 00 to 11 to 10 to 01 back to 00 and repeats.

7. What are the conditions for the two machines are to be equivalent? For the machine given below, find the equivalence partition and a corresponding reduced machine in standard form:

PS	NS, Z	
	X=0	X=1
A	F, 0	B, 1
B	G, 0	A, 1
C	B, 0	C, 1
D	C, 0	B, 1
E	D, 0	A, 1
F	E, 1	F, 1
G	E, 1	G, 1

8. Construct an ASM block that has 3 input variables (D,E,F) and 4 output variables (P,Q,R,S) and 2 exit paths. For this block, output P is always 1, and Q is 1 if D=1. If D and F are 1 or if D and E are 0, R=1 and exit path 2 is taken. If (D=0 and E=1) or (D=1 and F=0), S=1 and exit path 1 is taken. Realize it with One flip flop per state.

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Code No: RR222201 **Set No.4**

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Time: 3 hours **Max Marks: 80**

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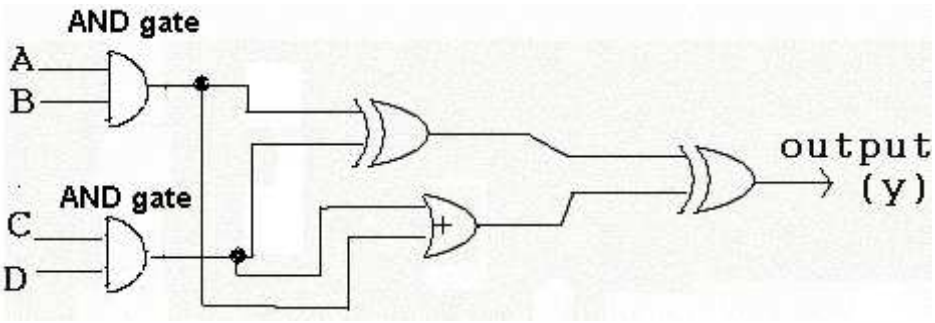
1. (a) Subtract in binary. Place a 1 over column from which it was necessary to borrow
   i. 11011011-1101101
   ii. 10001100-1100101
   iii. 11011101-11101010
   iv. 1000000000-0011111
   (b) Divide in binary:
   i. 10111101001
   ii. 1100000011110.

2. (a) i. Given $\overline{AB}+\overline{A}B = C$, Show that $\overline{AC}+\overline{A}C = B$.
   ii. $(A+B)\,(\overline{A}+C)(\overline{B}+D)\,(C+\overline{D})$; simplify
   (b) Define the connective * for the two valued variables A, B, and C as follows $A^*B = AB+\overline{AB}$
   Let $C = A^*B$, Determine which of the following is valid
   i. $A = B^*C$
   ii. $B = A^*C$
   iii. $A^*B^*C=1$

3. (a) Realize the given function using NAND-NAND and NOR-NOR two level logic and draw the circuit
   F= $X\overline{Y}Z + \overline{X}YZ + W$
   (b) Redraw the given circuit after simplification:



4. (a) Design 64 line output demultiplexer using lower order demultiplexer. Such as 4 to 16 and 2 to 4 Demultiplexers.

(b) Give the NAND gate realization of full-adder.

5. (a) Define a sequential system and how does it differ from a combinational system

   (b) Augment an S-R Flip-Flop with two AND gates to form a J-K-Flip-Flop and explain its operations with the help of Truth-Table

6. Design a counter which could count either in mod 8 straight binary or in mod 8 cyclic code based on a control signal.

7. For the machine shown in the table below obtain:

   (a) The corresponding reduced machine table in standard form

   (b) Find a minimum length that distinguishes state A from state B where PS: present state, NS: next state, Z: output, X: input

PS	NS, Z	
	X=0	X=1
A	B, 1	H, 1
B	F, 1	D, 1
C	D, 0	E, 1
D	C, 0	F, 1
E	D, 1	C, 1
F	C, 1	C, 1
G	C, 1	D, 1
H	C, 0	A, 1

8. Construct an ASM block that has 3 input variables (A,B,C), 4 output (W,X,Y,Z) and 2 exit paths. For this block, output Z is always 1, and W is 1 if A and B are both 1. If C=1 and A=0, Y=1 and exit path 1 is taken. If C=0 or A=1, X=1 and exit path 2 is taken.
   Realize the above using the One flip flop per state.

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