Code No: NR220203 **NR**

II B.Tech II Semester Supplementary Examinations, April/May 2005
LINEAR & DIGITAL IC APPLICATIONS
(Common to Electrical & Electronic Engineering and Electronics & Computer Engineering)

Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
All Questions carry equal marks

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1. (a) Why is emitter resistor R_E replaced by a constant current bias circuit in differential amplifier stage of an OP-AMP?
   (b) Explain why open loop configurations are not used in linear applications
   (c) For an OP-AMP, PSRR=70dB(min),CMRR=10^5,differential mode gainA_d=10^5. The output voltage changes by 20V in 4 microseconds. Calculate i)numerical value of PSRR ii) Common mode gain iii) Slew rate of the OP-AMP.

2. (a) Draw the circuit diagram and explain the operation of an inverting amplifier
   (b) Derive the output voltage of an OP-AMP based differential amplifier

3. (a) Derive the frequency of oscillation of a RC phase shift oscillator and explain the operation of the circuit.
   (b) Define supply voltage sensitivity. What is meant by poorly regulated power supply?

4. (a) Explain the operation of Astable multivibrator using 555 timer.
   (b) Design a square waveform generator of frequency 1kHz and duty cycle of 75% using 555 timer.

5. (a) Explain the terms Lock range, Capture range and Pull-in time a PLL. How are Lock Range and Capture range determined?
   (b) Design a PLL circuit using IC 565 to get
      i. Free-running frequency = 4.5 KHz
      ii. Lock range of 2 KHz and
      iii. Capture range = 100 Hz.

      Assume a supply voltage of + or - 10V. Show the circuit diagram with all component values.

6. (a) Explain the design procedure (with suitable circuit diagram of a fourth order Butterworth low-pass filter).
   (b) A certain narrow band-pass filter has been designed to meet the following specifications: f_C=$2kHz$. Q=20, and A_p=10. What modifications are necessary in the filter circuit to change the center frequency 'f_c' to $1kHz$, keeping the gain and band-width constant?

7. (a) List out the advantages of CMOS logic.
   (b) Draw the circuit of CMOS NOR gate and verify the Boolean function.
   (c) Give the working principle of I^2L logic with neat circuit diagram.
8. (a) Why successive approximation A/D converter faster than dual-slope A/D converter? Explain.
   (b) Draw the complete schematic circuit of successive approximations A/D converter and explain operations of this system.

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