Code No: OR220553 **OR**

II B.Tech II Semester Supplementary Examinations, April/May 2005
SWITCHING AND LOGIC THEORY THROUGH DIGITAL ICS
(Common to Computer Science & Engineering and Information Technology)

Time: 3 hours **Max Marks: 70**

Answer any FIVE Questions
All Questions carry equal marks

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1. (a) Draw the 2 input TTL NAND Gate and explain its operation.
   (b) Compare CMOS and TTL with respect to
      i. Propagation delay
      ii. Power dissipation
      iii. Fan-in, fan-out
      iv. Noise margin
      v. Speed power product
2. Simplify using K-map
   $f(a, b, c, d) = \sum (0, 2, , 6, 7, 8, 13) + \sum \phi(4, 10, 12)$
3. Simplify the following Boolean equation using Quin-MC cluskey method.
   $f(a, b, c, d) = \sum m(0, 2, 3, 6, 7, 8, 10, 12, 13)$
4. (a) Implement the following Boolean expression only with NAND Gates. $Y = A + \bar{B} + \bar{A}B$
   (b) Design a full adder circuit and implement it with only NOR Gate.
5. Design a 3 to 8 decoder circuit and Realize it. Give its truth table. Mention the digital IC version of that decoder.
6. (a) Distinguish between sequential and combinational logic circuits.
   (b) Develop a synchronous three bit up/down counter with a grey code sequence. The counter should count up when an up/down control input is 1 and count down when the control output is zero.
7. (a) Realize D Flip-Flop using JK Flip-Flop.
   (b) Realize a master slave JK Flip Flop using NAND gates and explain its operation and point out how race condition is avoided.
8. Draw a sequential detector which produces an output every time when the sequence 1101 is detected and an output 'O' at all other time Draw the state diagram as a design tool.

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