Code No: OR220554 **OR**

II B.Tech II Semester Supplementary Examinations, April/May 2005
COMPUTER ARCHITECTURE
(Computer Science & Engineering)

Time: 3 hours **Max Marks: 70**

Answer any FIVE Questions
All Questions carry equal marks

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1. Illustrate different addressing modes with suitable examples for each.
2. (a) Illustrate with suitable sketches, various IEEE standard floating -point formats.
   (b) Convert the numbers 16 and 11 into binary and perform multiplication using Booth algorithm.
3. Explain the steps and corresponding actions involved in the control sequence for execution of the following instructions.
   (a) Add (R3),R1
   (b) Move X(Rsrc),Rdst
4. (a) Distinguish the fixed point arithmetic followed in RISC and CISC processors.
   (b) Distinguish between hardwired control and micro-programmed control.
5. (a) What is the difference between a microprocessor and a micro program.
   (b) Give a brief note about the steps involved in the design of a micro programmed control unit.
6. (a) Distinguish between static and dynamic RAM.
   (b) Sketch the static RAM and dynamic RAM memory cells.
   (c) How many 512K x 8 memory chips are required to design a 2M x 32 memory module.
7. (a) Explain how direct mapping and associative mapping functions are implemented in cache memories.
   (b) What is virtual memory . Explain how the virtual memory address is translated to physical address in main memory.
8. (a) Give a brief note about the issues that are to be dealt while handling multiple I/O devices.
   (b) Sketch the timing diagram of an input transfer on a synchronous bus.

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