Code No: OR220451 **OR**

II B.Tech II Semester Supplementary Examinations, April/May 2005
SWITCHING THEORY & LOGIC DESIGN
(Common to Electronics & Communication Engineering, Electronics & Instrumentation Engineering, Electronics & Control Engineering and Electronics & Telematics)

Time: 3 hours **Max Marks: 70**

Answer any FIVE Questions
All Questions carry equal marks

⋆ ⋆ ⋆ ⋆ ⋆

1. (a) Perform the subtraction with the following unsigned binary numbers by taking the 2's complement of the subtrahend.
   i. 11010-10000
   ii. 11010-1101
   iii. 100-110000
   iv. 1010100-1010100
   (b) The binary numbers listed have a sign bit in the left most position and, if negative, are in 1's complement form. Perform the arithmetic operations indicated and verify the answers.
   i. 101011+111000
   ii. 001110+110010
   iii. 111001-001010
   iv. 101011-100110

2. (a) Find the minimal expression for the function f(w,x,y,z)=$\sum$(0,2,5,9,15) +$\sum$d (6,7,8,10,12,13) using Karnaughs-map.
   (b) i. Determine the Canonical sum-of-products form for $T(x, y, z) = \overline{x}y + \overline{z} + xyz$
   ii. Minimize the function $f(x, y, z, w) = x + xyz + wx + \overline{x}y + \overline{w}x + \overline{x}yz$.

3. (a) Implement the following function using only NOR gates F=a .(b+ c.d) + (b . $\overline{c}$).
   (b) Implement the following function using only NAND gates G=(a + $\overline{b}$). (c. d + $\overline{e}$)
   (c) Give the minimum two-level SOP realization of the following switching function using only NAND gates. F(x,y,z) = $\sum$ m (0,3,4,5,7)

4. (a) Design 4 to 6 decoder using 2 to 4 decoders and basic gates.
   (b) Implement Full adder circuit using ROM and Verify the working.

5. (a) Draw the circuit diagram of master slave J-K flip flop and explain its operation with the help of truth table. How it is different from edge triggering. Explain.
   (b) Give the transition table for the following flip flops.

i. RS flip flop
ii. J-K flip flop
iii. T flip-flop and
iv. D flip flop

6. Design a 4-bit universal shift register and draw the circuit with the given mode of operation table.

S_1	S_0	Operation
0	0	Parallel
0	1	Shift right
1	0	Shift left
1	1	Inhibit clock

7. For the machine shown in the table below obtain:
   (a) The corresponding reduced machine table in standard form
   (b) Find a minimum length that distinguishes state A from state B where PS: present state, NS: next state, Z: output, X: input

PS	NS,Z	
	X=0	X=1
A	B,1	H,1
B	F,1	D,1
C	D,0	E,1
D	C,0	F,1
E	D,1	C,1
F	C,1	C,1
G	C,1	D,1
H	C,0	A,1

8. Construct an ASM block that has 3 input variables (A,B,C), 4 output (W,X,Y,Z) and 2 exit paths. For this block, output Z is always 1, and W is 1 if A & B are both 1. If C=1 & A=0, Y=1 and exit path 1 is taken. If C=0 or A=1, X=1 and exit path 2 is taken. Realize the above using the multiplier and register.

⋆ ⋆ ⋆ ⋆ ⋆