Code No: NR310201 **NR**

III B.Tech I Semester Supplementary Examinations, May 2005
COMPUTER ORGANISATION
(Common to Electrical & Electronic Engineering, Electronics & Communication Engineering, Electronics & Instrumentation Engineering and Electronics & Telematics)

Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
All Questions carry equal marks

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1. (a) Perform the arithmetic operations (+70) + (+80) and (-70) + (-80) with binary numbers in 2s complement representation with 8-bits for binary representation including sign bit. Show that the overflow occurs in both cases.
   (b) Discuss about floating-point multiplications with a flow chart.
2. (a) Explain the stack oriented operations using a neat diagram.
   (b) Mention the different cache management instructions of POWER PC processor
3. (a) List the micro-operations required to carryout the following instructions. Assume a simple CPU with single accumulator.
      i. Load accumulator
      ii. Store accumulator
      iii. Add to accumulator
      iv. Complement accumulator
   (b) What is ICC? What for ICC is used?
4. Consider an accumulator based CPU with the following eight one address instructions. LOAD X, STORE X, ADD X, AND X, JMP X, JMPZ X, CMPL, (Complement Accumulator), and RSHIFT. Give fetch and execute cycle operations and identify the necessary control signals to be generated for the above instructions by a micro programmed control unit.
5. Write short notes on the following:
   (a) Look-aside organization for cache
   (b) Look-through organization for cache
6. (a) What are the advantages of paging?
   (b) Explain how the logical address can be converted into physical address in a paging system?
7. What is Asynchronous Data Transfer? Explain various methods of asynchronous data transfer with timing diagrams.
8. (a) Differentiate between programmed I/O and memory mapped I/O.

(b) Compare interrupt I/O control with DMA I/O control. Why does DMA have priority over CPU when both requests a memory transfer?

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