Code No: RR310201 **Set No.1**

III B.Tech. I Semester Supplementary Examinations, May -2005
COMPUTER ORGANIZATION
(Common to Electrical & Electronic Engineering, Electronics & Communication Engineering, Electronics & Instrumentation Engineering, Electronics & Telematics and Instrumentation & Control Engineering)
Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
All Questions carry equal marks

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1. (a) Explain about IAS memory formats.
   (b) List various registers in a computer along with their purpose
2. (a) Perform the subtraction on the following decimal numbers using 9s complement representation.
      i. 23-12
      ii. 23-29
   (b) A binary computer uses 36 bit registers to store numbers. Eight bits are used for the exponent and the exponent is represented in excess 64 form. Find the approximate range of decimal numbers handled by this computer
3. (a) List the instruction formats used on the PDP-11.
   (b) Draw and explain Pentium instruction format.
4. (a) Explain about the machine state register.
   (b) Discuss about the sequence of steps that occurs when an interrupt occurs
5. (a) Explain the cache execution of a write operation with a neat diagram
   (b) Elaborate on look-through organization for caches.
6. Discuss about data organization and formatting of magnetic disk in detail
7. (a) List and explain the functions of control unit
   (b) What is sequencing logic unit? Explain it's purpose.
8. (a) Give a summary of arithmetic and logical operations that are defined for the vector architecture.
   (b) What is cache coherence problem. Discuss about different cache coherance approches.

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Code No: RR310201 **Set No.2**

III B.Tech. I Semester Supplementary Examinations, May -2005
COMPUTER ORGANIZATION
(Common to Electrical & Electronic Engineering, Electronics & Communication Engineering, Electronics & Instrumentation Engineering, Electronics & Telematics and Instrumentation & Control Engineering)

Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
All Questions carry equal marks

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1. (a) Explain about IAS memory formats.
   (b) List various registers in a computer along with their purpose
2. Convert the following decimal numbers to base three and to base five.
   (a) 73
   (b) 10.333
   (c) 21.25
3. (a) Describe various Pentium data types
   (b) Describe various common data transfer instruction set operations.
4. (a) List the characteristics of superscalar processors and contrast it with CISC processors.
   (b) Explain the instruction execution characteristics of RISC processors.
   (c) What is semantic gap problem?
5. (a) Explain various schemes available for partitioning memory and the merits and demerits of each.
   (b) What is compaction
   (c) Differentiate between external and internal fragmentation
6. (a) List the hardware events that occur after an I/O device completes an I/O operation in interrupt driven I/O.
   (b) List and explain the interrupt modes of Intel 8259A interrupt controller.
7. Discuss about current applications of micro programming in detail.
8. (a) Classify and explain different multiprocessors
   (b) Explain the organization of tightly coupled multiprocessor system with a generic block diagram.

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Code No: RR310201 **Set No.3**

III B.Tech. I Semester Supplementary Examinations, May -2005
COMPUTER ORGANIZATION
(Common to Electrical & Electronic Engineering, Electronics & Communication Engineering, Electronics & Instrumentation Engineering, Electronics & Telematics and Instrumentation & Control Engineering)

Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
All Questions carry equal marks

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1. Explain about VonNeumann architecture design in detail.
2. (a) Explain the subtraction of numbers represented in floating point with example
   (b) Perform the following arithmetic operations assuming that the decimal digits are coded in 8421 code.
      i. 24 + 16
      ii. 84 - 97
3. (a) List the instruction formats used on the PDP-11.
   (b) Draw and explain Pentium instruction format.
4. (a) List the characteristics of superscalar processors and contrast it with CISC processors.
   (b) Explain the instruction execution characteristics of RISC processors.
   (c) What is semantic gap problem?
5. Explain different techniques of cache mapping function with merits and demerits of each.
6. Discuss three possible techniques for I/O operations with merits and demerits of each.
7. (a) Differentiate between micro programmed and hard wired control units with merits and demerits of each.
   (b) Discuss about the design considerations of micro instruction sequencing technique.
8. (a) Elaborate on continuous field simulation problems.
   (b) Discuss the organization of IBM 3090 with vector facility.

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Code No: RR310201 **Set No.4**

III B.Tech. I Semester Supplementary Examinations, May -2005
COMPUTER ORGANIZATION
(Common to Electrical & Electronic Engineering, Electronics & Communication Engineering, Electronics & Instrumentation Engineering, Electronics & Telematics and Instrumentation & Control Engineering)
Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
All Questions carry equal marks

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1. (a) Discuss the interconnection structure design of a computer.
   (b) Explain various bus lines.
   (c) What do you mean by multiple - bus hierarchies.
2. (a) Explain the subtraction of binary numbers in twos complement notation
   (b) Discuss about floating point addition.
3. NOOP instruction has no effect on the CPU state other than incrementing the program counter. Suggest some uses of this instruction with examples.
4. (a) Explain about the machine state register.
   (b) Discuss about the sequence of steps that occurs when an interrupt occurs
5. (a) Explain the principles of segmentation .
   (b) Discuss about address translation in segmentation.
   (c) What is hit ratio?
6. (a) List the major functions of disk controller.
   (b) Explain about disk arrays.
   (c) Differentiate between Winchester disks and floppy disks.
7. (a) Discuss about the evolution of I/O function.
   (b) Explain the characteristics of I/O channels.
8. (a) Discuss about flow of instruction execution unit pipelined processors.
   (b) Explain the factors affecting throughput in pipelined processors.

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