Code No: RR310401 **Set No.1**

III B.Tech. I Semester Supplementary Examinations, May -2005
DIGITAL IC APPLICATIONS
(Electronics & Communication Engineering)

Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
All Questions carry equal marks

⋆ ⋆ ⋆ ⋆ ⋆

1. (a) Design a three input NAND gate using diode logic and a transistor inverter? Analyze the circuit with the help of transfer characteristics?
   (b) Design a CMOS transistor circuit with the functional behavior f(X)=$\overline{(A+\bar{B})(B+\bar{D})(A+\bar{D})}$
2. (a) Draw the circuit diagram of basic CMS gate and explain the operation?
   (b) List out different categories of characteristics in a TTL data sheet? Discuss electrical and switching characteristics of 74LS00.
3. (a) Explain the behavioral design model of VHDL?
   (b) Design the logic circuit and write a data-flow style VHDL program for the following function?
   F (X) = $\Sigma_{A,B,C,D}$ (3,5,6,7,13) + d(1,2,4,12,15)
4. (a) Write a VHDL program for 74×245?
   (b) Design a 16-bit comparator using 74×85 Ics?
5. Draw the logic diagram of 74×283 IC and explain the operation? Write data flow VHDL program for this IC?
6. (a) Distinguish between latch and flip-flop? Show the logic diagram for both? Explain the operation with the help of function table?
   (b) Design a conversion circuit to convert a T flip-flop to J-K flip-flop?
7. (a) What is the difference between ring counter and Johnson ring counter? Design a self-correcting 4-bit, 4-state ring counter with a single circulating 0 using 74x194?
   (b) Define clock skew? Explain how clock skew leads to incorrect outputs in synchronous circuits? Design one logic circuit that minimizes clock skew?
8. (a) With the help of timing waveforms, explain read and write operations of static SRAM?
   (b) Explain XC4000 programmable interconnect structure?

⋆ ⋆ ⋆ ⋆ ⋆

Code No: RR310401 **Set No.2**

III B.Tech. I Semester Supplementary Examinations, May -2005
DIGITAL IC APPLICATIONS
(Electronics & Communication Engineering)

Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
All Questions carry equal marks

⋆ ⋆ ⋆ ⋆ ⋆

1. (a) Design a CMOS transistor circuit with the functional behavior f(X) = $\overline{(A+\bar{B})(C+\bar{D})}$
   (b) Distinguish between static and dynamic power dissipation of a CMOS circuit? Derive the expression for dynamic power dissipation?
2. (a) Design a TTL three-state NAND gate and explain the operation with the help of function table?
   (b) Explain the following terms with reference to TTL gate?
      i. Logic levels
      ii. DC Noise margin
      iii. Low-state unit load
      iv. High-state fanout
3. (a) What is the importance of time dimension in VHDL and explain its function?
   (b) Design the logic circuit and write a data-flow style VHDL program for the following function?
   F (X) = $\Sigma_{A,B,C,D}$ (0,1,3,5,14) + d(8,15)
4. (a) Give the logic diagram of 74×139? Explain with the help of truth table? Using this device design a 3 to 8 decoder and provide the truth table?
   (b) Design a 16-bit comparator using 74×85 Ics?
5. (a) Design a full subtractor with logic gates and write VHDL data flow program for the implementation of the above subtractor?
   (b) Using the above subtractor design a 8-bit ripple subtractor and write the corresponding VHDL program?
6. With the help of logic diagram explain the function of PAL16R6? Explain how an 8-bit synchronous binary counter can be realized with this device?
7. (a) Design an 8-bit parallel-in and parallel-out shift register and explain the operation?
   (b) Write data-flow style VHDL program for the above circuit?
8. (a) Explain the internal structure of 64Kx1 DRAM? With the help of timing waveforms discuss DRAM access?
   (b) With a neat sketch, explain the general architecture of FPGA chip? What is the importance of configurable logic block?

⋆ ⋆ ⋆ ⋆ ⋆

Code No: RR310401 **Set No.3**

III B.Tech. I Semester Supplementary Examinations, May -2005
DIGITAL IC APPLICATIONS
(Electronics & Communication Engineering)

Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
All Questions carry equal marks

⋆ ⋆ ⋆ ⋆ ⋆

1. (a) Design a three input NAND gate using diode logic and a transistor inverter? Analyze the circuit with the help of transfer characteristics?
   (b) Compare HC, HCT, VHC and VHCT CMOS logic families with the help of output specifications with V_{CC} from 4.5V to 5.5V?
2. (a) Mention the DC noise margin levels of ECL 10K family?
   (b) A single pull-up resistor to +5V is used to provide a constant-1 logic source to 15 different 74LS00 inputs. What is the maximum value of this resistor? How much high state DC noise margin can be provided in this case?
3. (a) Explain data-flow design elements of VHDL?
   (b) Write a data-flow style VHDL program for the following functions?
   F(S) = A $\oplus$B$\oplus C_I$
   F(C_O) = $AB + AC_I + BC_I$
4. (a) Draw the digits created by 74x49 seven-segment decoder for non-decimal inputs 1010 through 1111?
   (b) Realize the following expression using 74×151 IC
   f (X) = $\bar{A}BC + A\bar{B}C + AB\bar{C}$
5. A 16-bit barrel shifter is a combinational logic circuit with 16-data inputs, 16-data outputs and 4-control inputs. The input word is rotated by a number of bit positions specified by control bits. Write a VHDL program for the above implementation?
6. (a) Discuss the logic circuit of 74×377 register? Write a VHDL program for the above logic?
   (b) Design a modulo-64 counter using 74×163 ICs?
7. (a) Draw the logic diagram of 74x194 and explain the operation?
   (b) Design a serial binary adder? Develop the VHDL program for simulating serial binary adder?
8. (a) Explain the operation of Synchronous SRAM with the help of its internal architecture?
   (b) Determine the ROM size needed to realize the logic function performed by 74x153 and 74x139?

⋆ ⋆ ⋆ ⋆ ⋆

Code No: RR310401 **Set No.4**

III B.Tech. I Semester Supplementary Examinations, May -2005
DIGITAL IC APPLICATIONS
(Electronics & Communication Engineering)

Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
All Questions carry equal marks

⋆ ⋆ ⋆ ⋆ ⋆

1. (a) Draw the transistor logic inverter circuit and analyze the circuit behavior with the help of transfer characteristics?
   (b) Design a CMOS transistor circuit that has the functional behavior
   f (Z) = $\overline{(A + \bar{B})(B + C)}$
2. (a) Design a transistor circuit of 2-input ECL NOR gate? Explain the operation with the help of function table?
   (b) Compare CMOS, TTL and ECL with reference to logic levels, DC Noise margin, propagation delay and fanout?
3. (a) What is the importance of time dimension in VHDL and explain its function?
   (b) Design the logic circuit and write a data-flow style VHDL program for the following function?
   F (X) = $\Sigma_{A,B,C,D}$ (0,1,3,5,14) + d(8,15)
4. (a) Realize the following expression using 74×151 IC
   f (Y) = AB + BC + AC
   (b) Write a data flow style VHDL program for a simple 8-bit multiplexer?
5. (a) Show the logic diagram of 74×283 binary adder? Explain the principle of generating sum and carry at every stage using the logic diagram?
   (b) Design a 24-bit group ripple adder using 74×283 Ics?
6. (a) Design a 4-bit binary synchronous counter using 74×74? Write VHDL program for this logic?
   (b) Design a modulo-60 counter using 74×163 ICs?
7. (a) What is the difference between ring counter and Johnson ring counter? Design a self-correcting 4-bit, 4-state ring counter with a single circulating 0 using 74x194?
   (b) Design a 3-bit LFSR counter using 74x194? List out the sequence assuming that the initial state is 101?
8. (a) Draw the basic cell structure of Dynamic RAM? What is the necessity of refresh cycle? Explain the timing requirements of refresh operation?
   (b) Discuss in detail ROM access mechanism with the help of timing waveforms?

⋆ ⋆ ⋆ ⋆ ⋆