Code No: OR310451 **OR**

III B.Tech I Semester Supplementary Examinations, May 2005
PULSE AND DIGITAL CIRCUITS
(Common to Electronics & Communication Engineering, Electronics & Instrumentation Engineering and Electronics & Control Engineering)
Time: 3 hours **Max Marks: 70**

Answer any FIVE Questions
All Questions carry equal marks

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1. (a) A pulse is applied to a low-pass RC circuit. Prove by direct integration that the area under the pulse is same as the area under the output waveform across the capacitor. Explain the result.
   (b) Write a short notes on Highpass RC circuit as a differentiator.
2. (a) Draw the circuit diagram of slicer circuit using Zener diodes and explain its operation with the help of its transfer characteristic.
   (b) For the circuit shown in figure 1 below:

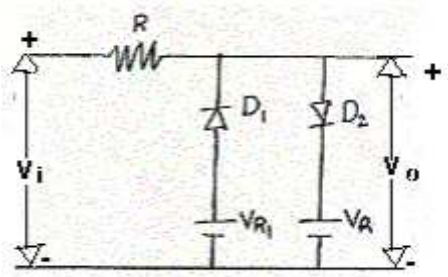

Figure 1:

If R = 1KΩ, V_{R2} = 10V, V_{R1} = 7 V
R_f = 0 and R_r =∝

   i. Sketch the transfer characteristic
   ii. If V_i = 20 sin ωt sketch the input and output waveforms.

3. (a) Explain the phenomenon of "latching" in a transistor switch.
   (b) A transistor has f_T = 50 MHz, 4_{FE}=40, $C_{b'c}$=3PF and operates with V_{cc}=12 V and R_c=500 Ω. The transistor is operating initially in the neighbourhood of the cut-in point. What base current must be applied to drive the transistor to saturation in 1μ sec?
4. (a) Draw the circuit diagram of self-bias with symmetrical triggering using diodes. Explain the working of the same.
   (b) Compare between triggering at base and collectors.
5. (a) Define the three errors that occur in a sweep circuit and obtain an expression for these errors for an exponential sweep circuit.

(b) Explain with a circuit the working of a UJT sweep circuit and obtain the expressions for the intrinsic stand off ratio (η).

6. (a) Bring out the importance of synchronization and frequency division.

   (b) The relaxation oscillator when running freely, generates an output sweep amplitude of 100V and frequency 1kHz. Synchronizing pulses are applied such that at each pulse the breakdown voltage is lowered by 20V. Over what frequency range may the synchronizing pulse frequency be varied if 1:1 synchronization is to result?

7. (a) Illustrate with neat circuit diagram, the operation of unidirectional sampling gate for multiple inputs.

   (b) Explain with circuit diagram the operation of a two input sampling gate which does not have any loading effect on control signal.

8. Explain the operation of an RC controlled free running blocking oscillator with neat sketch of circuit and voltage waveforms. Derive the expression for duty cycle. What are the advantages of the circuit?

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