Code No: RR311901 **Set No.1**

III B.Tech. I Semester Supplementary Examinations, April/May -2005
DIGITAL SYSTEMS DESIGN
(Electronics & Computer Engineering)

Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
All Questions carry equal marks

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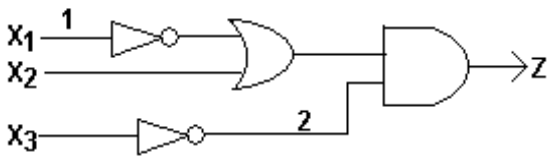
1. (a) Draw a ASM chart the specify a conditional operation to increment register R during state T_1 and transfer to state T_2 if control inputs z and y are equal to 1 and zero, respectively.
   (b) Derive the PLA programming table for the combinational circuits that square a 3-bit number. Minimize the number of product terms.

2. (a) How is an essential prime cube detected in
      i. The Quine-Mc Cluskey method.
      ii. The adjacency method and
      iii. CAMP algorithm.
   (b) Determine if the cubes 0221 and 2122 are wholly with in the function.

3. (a) What do you mean by a fault in a circuit? How do you classify the faults in a circuit? Explain them.
   (b) Using Boolean difference method, find the test vectors for SAO fault on input line 1 and SAI on the internal line 2 of the circuit shown below.



4. (a) Prove that the length L of the minimal distinguishing sequence for a machine with n state and q output symbols is bounded by $L \geq \frac{\log_2 n}{\log_2 q}$.
   (b) Describe the second algorithm for the design of fault detection experiment.

5. (a) Suggest an improvement over the control input procedure or entirely new method without using a shift register such that a PLA can be made completely testable in the presence of a masking cycle?
   (b) What are the various DFT scheme? Explain one technique with an example.

6. (a) State and prove EPC test Criteria.
   (b) Explain in detail about ASIC and its applications.

7. (a) Describe the various faults in PLAs.
   (b) Explain the fault detection by path-sensitization. Procedure.
8. Write notes on:
   (a) Built-in-self Test
   (b) Test generation
   (c) PLA folding.

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Code No: RR311901 **Set No.2**

III B.Tech. I Semester Supplementary Examinations, April/May -2005
DIGITAL SYSTEMS DESIGN
(Electronics & Computer Engineering)

Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
All Questions carry equal marks

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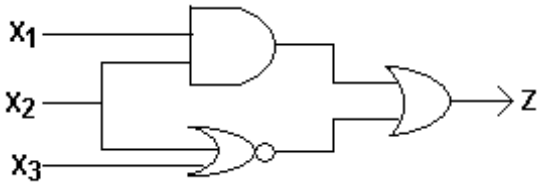
1. (a) Explain how the ASM chart differs from a conventional flow chart.
   (b) Show the 8 exit paths in an ASM block emanating from the decision boxes that check the 8 possible binary valves of 3-control variables x, y and z.

2. Construct 4-Variable Boolean functions whose processing by the CAMP algorithm involves the following. If impossible, explain why.
   (a) Generation of single-row MAM
   (b) Generation of a single-row MUM
   (c) Generation of a single row MAM and a single row MUM
   (d) Branching twice.

3. (a) Find the test vectors of all SAO and SAI faults of the circuit given below by Kohavi algorithm.



   (b) Explain how a fault in a circuit is diagnosed also describe the testing process.

4. (a) Describe the procedure to be employed for any machine that has a distinguishing sequence with repeated symbols.
   (b) Prove that every n-state machine has an adaptive homing sequence whose length is at most (n-1)n/2.

5. (a) Plot the following PLA on the map. Identify the undetectable faults.

x_1	x_2	x_3	x_4	x_5	x_6
0	2	2	1	1	0
2	1	1	2	1	1
0	1	2	1	0	1

   (b) How do you detect a specific fault? Explain.

6. (a) Describe the inadequacy of the minterm-based algorithm.

(b) With neat diagram describe fault-tolerant VLSI processor arrays.

7. (a) With illustrations describe undetectable faults.

   (b) Explain the properties of Boolean differences. Find the test vector to detect the fault SAO in the variable A of the given function $f = \overline{A}B + AC + BC$ using Boolean difference method.

8. Write notes:

   (a) DFT schemes.

   (b) CC Ds.

   (c) Failure Tolerant design.

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Code No: RR311901 **Set No.3**

III B.Tech. I Semester Supplementary Examinations, April/May -2005
DIGITAL SYSTEMS DESIGN
(Electronics & Computer Engineering)

Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
All Questions carry equal marks

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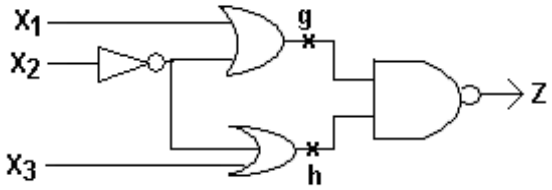
1. (a) Construct an ASM chart for digital system that counts the number of students in a classroom. The students enter the room from one door with photocell that changes a signal × from 1 to 0 when the light is interrupted. They leave the room from second door with a similar photocell with a signal y. Both x and y are synchronized with the clock, but they may stay on or off for more than one clock-pulse period. The data processor subsystem consists of an updown counter with a display of its contents.
   (b) Draw an ASM chart for binary multiplier.
2. (a) Discuss cube based algorithms giving examples.
   (b) Explain the various cubical operations.
3. (a) Describe a fault-table method for testing a circuit.
   (b) Derive by the path sensitization method the test vectors for SAO and SAI faults at g and h in the network shown below.



4. (a) Find a preset distinguishing experiment that determines the initial state of the machine shown below, given that it cannot be initially in state E.
   (b) Can you initial state when the initial uncertainty is (A B C D E)?

PS	NS,Z	
	X=0	X=1
A	B,1	A,1
B	E,0	A,1
C	A,0	E,1
D	C,1	D,1
E	E,0	D,1

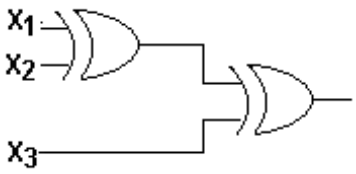
5. (a) With the help of a map, determine a minimal test set of the following PLA. List the undetectable faults.

(b) Discuss the major goals of testable designs.

X_1	X_2	X_3	X_4	Z_1	Z_2	Z_3
1	1	0	2	0	1	0
2	1	0	2	1	0	1
1	0	2	2	0	1	1
0	0	2	1	1	1	0

6. (a) The cubical form of a Boolean function is as follows
f = 0112 + 1221 + 2112
Find all the inter sectoring pairs of cubes without the help of a map.

(b) In the 3-bit parity checker circuit find the test vectors for SAO and SAI faults one each line of the circuit, using path-sensitization method.



7. (a) With necessary illustrations explain masking cycle for a PLA.

(b) For the following machine determine whether or not preset distinguishing sequence exists, if any do exists, find the shortest one.

PS	NS,Z	
	x=0	x=1
A	D,0	C,1
B	A,0	B,1
C	E,0	B,1
D	B,0	D,1
E	C,1	E,1

8. Write notes on:

(a) Test generation

(b) Built-in-self test

(c) Bubble memories.

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Code No: RR311901 **Set No.4**

III B.Tech. I Semester Supplementary Examinations, April/May -2005
DIGITAL SYSTEMS DESIGN
(Electronics & Computer Engineering)

Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
All Questions carry equal marks

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1. Obtain the ASM Charts for the following state transitions:
   (a) If x = 0, Control goes from state T_1 to state T_2, if x = 1, generates a conditional operation and go from T_1 to T_2.
   (b) If x = 1, control goes from T_1 to T_2 and then to T_3, If x = 0, control goes from T_1 to T_3.
   (c) Start from state T_1; Then; if xy = 00, go to T_2; if xy = 01, go to T_3; if xy =10, go to T_1; otherwise, go to T_3.

2. (a) With the help of a map, find the CAMP print out of the following cyclic functions. After branching, how many times, and out which minterms, will the programme fail to get a VSPC and therefore skip the minterms? The function will be input in the same order as given in the function, f(a b c d) = Σ (0, 1, 3, 5 8, 10 14).
   (b) How is a redundant prime cube is detected in CAMP algorithm?

3. (a) Explain in detail adaptive experiments with an example to diagnose faults in circuit.
   (b) A Circuit realizes the function $Z = x_1'x_4 + x_2'x_3 + x_1x_4'$. Using Boolean difference method, find the test vectors for SAO and SAI faults on all input lines of the Circuit.

4. (a) What is a diagnosable machine? Explain the design method of definitely diagnosable machine.
   (b) Prove that, in a reduced n-state machine, every set of n-k states ($n-2 \geq K \geq 0$) contains a least one pair of states which is distinguishable by an experiment of length K+1.

5. (a) What is the need of Built-in-Self-Test (BIST)? Discuss "ignature analysis" with a neat diagram.
   (b) With the help of a map, determine the minimal test for the following PLA. List undetectable faults, if any.

x_1	x_2	x_3	x_4	z_1	z_2
1	2	0	1	1	0
2	0	1	1	1	0
1	1	0	2	1	1
0	1	1	0	0	1

6. (a) With the help of a map, calculate DA and SSM of minterms 2,4,12 and 15 in the following function:
   $f = \sum (2-4, 6-8, 12, 15) + \phi \sum (5, 11, 13)$
   (b) Describe PLA folding algorithm.

7. (a) List the PLA programming table for BCD-to-excess-3 code converter.
   (b) Describe the fault-tolerant VLSL processor array.

8. Write notes on:
   (a) Kohavi algorithm
   (b) FPGA
   (c) PLA minimization.

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