Code No: NR320404 **NR**

**III B.Tech II Semester Supplementary Examinations, April/May 2005**
**VLSI TECHNOLOGY**
**( Common to Electronics & Communication Engineering and Electronics & Telematics)**

**Time: 3 hours** **Max Marks: 80**

**Answer any FIVE Questions**
**All Questions carry equal marks**

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1. (a) Explain in detail the p-well process for CMOS fabrication indicating the masks used.
   (b) Draw a neat sketch of CMOS inverter fabricated using n-well process.
2. (a) Explain inverter delays for :
      i. Basic 4:1 n MOS inverter
      ii. Minimum size C MOS inverter
   (b) Derive an expression for the rise time and fall time of a C MOS inverter and explain the factors affecting these quantities
3. (a) Explain the sea of gates (SOG) structure and its advantages with suitable diagrams.
   (b) Compare and contrast standard cell design with gate array architecture?
4. (a) With the help of a block diagram explain the working of FPGA
   (b) What are the differences in design approach in the case of ASIC design and semi custom Design
5. Taking 4 bit ALU as an example , give the behavioural synthesis in VHDL.
6. Discuss the following types of simulations
   (a) circuit level
   (b) logic level
   (c) switch level
   (d) mixed mode and
   (e) timing simulations
7. (a) How packaging is affects on the performance of VLSI chip?
   (b) Explain surface mounting type packages.
8. (a) What are the key aspects of switch capacitor?
   (b) What are the different methods to design switched capacitor filters in VLSI.

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