Code No: NR321502 **NR**

III B.Tech II Semester Supplementary Examinations, April/May 2005
ADVANCED COMPUTER ARCHITECTURE
(Computer Science & Systems Engineering)

Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
All Questions carry equal marks

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1. (a) Differentiate among pipline, array and multiprocessor systems.
   (b) Explain serial versus parallel processing
2. (a) What is vector processing? Explain the important characters of vector processing.
   (b) Explain different fields of a vector Instructions.
3. (a) Construct of mesh connected an ILLiac-IV Network with N = 16 PE's. What is its equivalent chordal ring topology.
   (b) List down the various routing functions that characterizes Illiac − IV Network
4. (a) Describe M(j,k) sorting algorithm.
   (b) Describe a Bit serial Associative memory organization with suitable diagram
5. (a) Describe a multiport memory with private memories
   (b) Discuss how 1-by-8 demultipluxer is derived from 2x2 switches.
   (c) Give the circual diagram of a Buffered 2x2 crossbar
6. (a) What is meant by cache coherence? Explain how this problem can be avoided.
   (b) Derive an expression for processor utilization U, for the multiprocessor system with set-associative caches.
7. (a) Explain the VLSI arithmetic module for the multiplication of the sequences of 2 x 2 matrices.
   (b) Explain the principles of a pipelined VLSI matrix inverter.
8. (a) Give architecture of the front-end system interface with Cray-1 memory and functions sections.
   (b) Briefly explain the architecture of Cyber-205.

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