Code No: OR320456 **OR**

III B.Tech II Semester Supplementary Examinations, April/May 2005
VLSI TECHNOLOGY
(Electronics & Communication Engineering)

Time: 3 hours **Max Marks: 70**

Answer any FIVE Questions
All Questions carry equal marks

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1. Describe the constructional features and performance characteristics of
   (a) Psedo-n MOS Logic
   (b) Clocked CMOS Logic.
2. (a) Draw an n MOS transistor model indicating all parameters.
   (b) Draw the circuit diagram of a Bi CMOS inverter with no static current.
   (c) What is latch up incase of CMOS circuits ? Explain with relevant diagrams. How latch up problem can be overcome ?
3. (a) Give the cell description of an inverter.
   (b) Describe channel less gate arrays.
4. (a) Discuss in detail semi-custom layout styles.
   (b) Explain in detail about the configurable logic blocks.
5. (a) Explain about Automatic test vector generation.
   (b) How fault simulation is done and explain fault models with the help of examples.
6. Discuss the following types of simulations
   (a) circuit level
   (b) logic level
   (c) switch level
   (d) mixed mode and
   (e) timing simulations
7. (a) Why package is necessary for the VLSI Chip ?
   (b) What are the different package mounts and explain in brief
8. (a) Prove that the combination of BJT and MOS technology offers the best performance in Analog VLSI design.
   (b) Draw the block diagram of D/A converter suitable for VLSI Analog Circuits and explain.

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