Code No: OR320551 **OR**

III B.Tech II Semester Supplementary Examinations, January 2005
FAULT TOLERANT SYSTEMS
(Common to Computer Science & Engineering and Information Technology)

Time: 3 hours **Max Marks: 70**

Answer any FIVE Questions
All Questions carry equal marks

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1. Define and derive the following terms in a system:
   (a) MTTR
   (b) Hazard rate functions.
2. (a) What are the goals of design for stability?
   (b) Distinguish between deterministic test pattern generation and probabilistic test pattern generation methods.
3. (a) Design a redundant circuit for f = ab + $a^{/}b^{/}$.
   (b) Explain the Dynamic redundancy Technique of a fault Tolerant system.
4. (a) With an example explain the practical fault tolerant system?
   (b) How do you enhance the fault tolerance characteristics of digital systems.
5. (a) Design a totally self checking checker circuit using Maurf and Friedman method of realization.
   (b) Compare Berger codes with low cost residue codes in all aspects.
6. Explain the steps to derive G-functions which generates the $C_i(o \leq i \leq m)$ check bits in modified Berger code specially for detecting uni-directional output errors in PLAs. Take an example to explain the above steps.
7. (a) Prove that five tests are sufficient to detect all faults in a combinational logic circuit by inserting addition control logic to the following function, obtain the test pattern. $f = (A, B, C, D) = \overline{AB} + \overline{BC} + BD$
   (b) Obtain the ten sequences denoted as P = $x_o x_1 \ldots\ldots\ldots x_a$ from the basic module of the above circuit and get the compatable pair from the set P.
8. (a) Distinguish between single and double batch LSSD.
   (b) Explain the single latch LSSD design using the modified shift register latch to reduce the overhead

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