Code No: RA310401 **RA**

III B.Tech II Semester Regular Examinations, April/May 2005
DIGITAL IC APPLICATIONS
(Electronics & Communication Engineering)

Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
All Questions carry equal marks

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1. Design a CMOS transistor circuit with the functional behavior
   f(X) = $\overline{(A+\bar{B})(B+C+\bar{D})(A+\bar{D})}$
2. (a) What is the necessity of separate interfacing circuit to connect CMOS gate to TTL gate? Draw the interface circuit and explain the operation?
   (b) Draw the circuit diagram of basic CMS gate and explain the operation?
3. (a) Explain data-flow design elements of VHDL?
   (b) Write a data-flow style VHDL program for the following functions?
   F(S) = A $\oplus$B$\oplus C_I$
   F(C_O) = $AB + AC_I + BC_I$
4. (a) Using two 74×138 decoders design a 4 to 16 decoder?
   (b) Write a data flow style VHDL program for the above design?
5. (a) Design a full adder using two half adders? Write VHDL data flow program for the above implementation?
   (b) Design a 4×4 combinational multiplexer and write the corresponding VHDL program?
6. (a) Design a conversion circuit to convert a T flip-flop to J-K flip-flop? Write a data-flow VHDL program?
   (b) With the help of logic diagram discuss PAL16R8?
7. (a) Design an 8-bit parallel-in and parallel-out shift register and explain the operation?
   (b) What is the difference between ring counter and Johnson ring counter? Design a self-correcting 4-bit, 4-state ring counter with a single circulating 0 using 74×194?
8. (a) Determine the ROM size needed to realize the logic function performed by 74x153 and 74x139?
   (b) With a neat diagram explain the general architecture of CPLD? Discuss the key features of Xilinx XC9500 CPLD family?

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