Code No: RR320405 **Set No.1**

III B.Tech. II Semester Regular Examinations, April/May -2005
VLSI DESIGN
(Common to Electronics & Communication Engineering and Electronics & Telematics)

Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
All Questions carry equal marks

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1. (a) With neat sketches explain the formation of the inversion layer in P-channel Enhancement MOSFET.
   (b) An NMOS Transistors is operated in the triode region with the following parameters $V_{GS} = 4V$; $V_{tn} = 1V$; $V_{DS} = 2V$; $W/L = 100$; $\mu nCox = 90\ A/V^2$ Find its drain current and drain source resistance.
2. With neat sketches explain BICMOS fabrication in an n-well process.
3. Design a stick diagram for the CMOS logic shown below $Y = \overline{(A + B + C)}$
4. Design a layout diagram for the PMOS logic shown below $Y = \overline{(AB) + (CD)}$
5. Calculate the gate capacitance value of $5\mu m$ technology minimum sized transistor with gate to channel capacitance value is $4 \times 10^{-4} pF/\mu m^2$
6. Implement JK flip flop using PROM.
7. Explain clearly about the following
   (a) Technology independent logic optimization.
   (b) Technology dependent logic optimization.
8. Mention the properties of the twin oxide.

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Code No: RR320405 **Set No.2**

III B.Tech. II Semester Regular Examinations, April/May -2005
VLSI DESIGN
(Common to Electronics & Communication Engineering and Electronics & Telematics)

Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
All Questions carry equal marks

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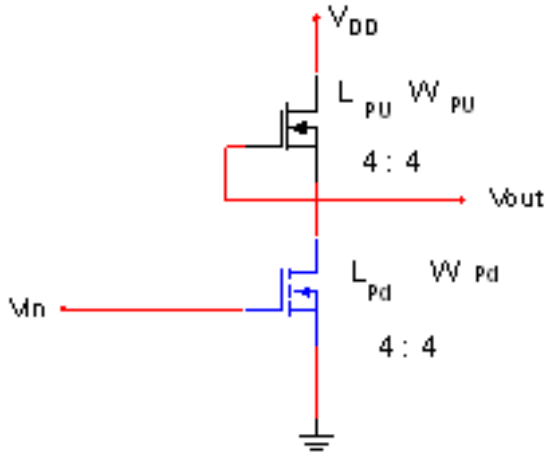
1. Explain with neat sketches the Drain and Transfer characteristics of p-channel enhancement MOSFET.
2. With neat sketches explain how Diodes and Resistors are fabricated in CMOS process.
3. Design a stick diagram for the CMOS logic shown below $Y = \overline{(AB + CD)}$
4. Design a layout diagram for two input pMOS NOR gate.
5. Calculate ON resistance from V_{DD} to GND for the given inverter circuit. If n-channel sheet resistance is $3 \times 10^4 \Omega$ per square.



6. Implement 2-bit comparator using PROM.
7. With respect to synthesis process explain the following terms.
   (a) Flattening
   (b) Factoring.
   (c) Mapping.
8. Clearly explain the wire bonding technology of the die bonding.

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Code No: RR320405 **Set No.3**

III B.Tech. II Semester Regular Examinations, April/May -2005
VLSI DESIGN
(Common to Electronics & Communication Engineering and Electronics & Telematics)

Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
All Questions carry equal marks

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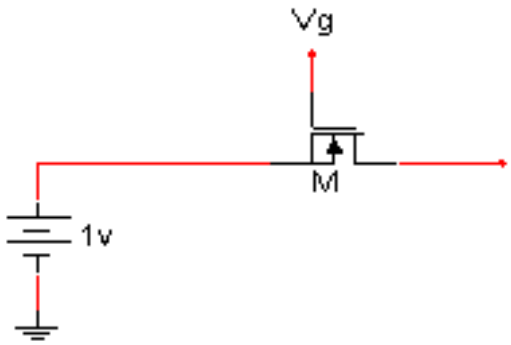
1. (a) Derive an equation for Transconductance of an n-channel enhancement MOSFET operating in Active region.
   (b) For the arrangement shown below plot the on-resistance of M as a function of V_G. Assume Vtn = 0.7 V; W/L = 10; μnCox = 50μA/V^2
   Note the drain terminal is open.



2. Compare between CMOS an bipolar technologies.
3. Design a stick diagram for the NMOS logic shown below $Y = \overline{(A+B).C}$
4. Design a layout diagram for the CMOS logic shown below $Y = \overline{(A+B).(C+D)}$
5. Calculate the gate capacitance value of $2\mu m$ technology minimum size transistor with gate to channel capacitance value is $8 \times 10^{-4} pF/\mu m^2$
6. Implement 2-bit comparator using PROM.
7. What are the different report files that are provided by the place and route tool and discuss clearly about each report file.
8. With neat sketches explain the electron lithography process.

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Code No: RR320405 **Set No.4**

III B.Tech. II Semester Regular Examinations, April/May -2005
VLSI DESIGN
(Common to Electronics & Communication Engineering and Electronics & Telematics)

Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
All Questions carry equal marks

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1. (a) With neat sketches explain the Drain characteristics of the p-channel Enhancement MOSFET
   (b) An p-MOS Transistor is operated in the Active region with the following parameters $V_{GS} = -4.5V$; $V_{tp} = -1V$; $W/L = 95$; $\mu nCox = 95\ \mu A/V^2$ Find its drain current and drain source resistance.
2. With neat sketches explain CMOS fabrication using p-well process.
3. Design a stick diagram for the CMOS logic shown below $Y = \overline{(A+B).C}$
4. Design a layout diagram for the PMOS logic shown below $Y = \overline{(AB)+(CD)}$
5. Explain clearly about different parastic capacitances of an nMOS transistor.
6. With neat sketches explain the architecture of PAL.
7. What are the different inputs that are provided to the place and route tool and explain the significance of each input.
8. Clearly explain the diffusion process in IC fabrication.

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