Code No: RR321202 **Set No.1**

III B.Tech. II Semester Regular Examinations, April/May -2005
VLSI SYSTEMS DESIGN
(Information Technology)

Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
All Questions carry equal marks

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1. Implement the following logic functions using CMOS logic
   (a) $Y = \{A.B.C.D\}^1$
   (b) $Y = \{A + B + C + D\}^1$
2. Name different IC fabrication technologies with suitable examples.
3. Design a stick diagram for two-input N-MOS NAND and NOR gates.
4. (a) What do you mean by layout of a component?
   (b) Draw neat layout diagram for NMOS transistor
5. Define faults of a Digital circuit and Explain about struck at 0 /1 faulty models
6. Draw the circuit diagram of Depletion-load NMOS SRAM cell and explain its working principle.
7. Clearly explain about block placement and channel definition with respect to floor planning of the chip.
8. Write a register-transfer description of one four-digit timer.

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Code No: RR321202 **Set No.2**

III B.Tech. II Semester Regular Examinations, April/May -2005
VLSI SYSTEMS DESIGN
(Information Technology)

Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
All Questions carry equal marks

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1. Implement the following gates with p-MOS transistors only and explain its working
   (a) 2 Input AND gate.
   (b) 4 Input NOR gate.
2. An n-MOS transistor is operating in the triode region with the following parameters $\mu_n Cox = 90\mu\ A/V^2$ W/L (ratio) = 100 $V_{gs} = 4V,\ V_{tn} = 1V,\ V_{ds} = 2V$. Find its drain current & drain -Source resistance.
3. Explain with neat sketches CMOS fabrication using n - well process.
4. Implement EX-OR and EX-NOR gates using static complementary logic.
5. (a) With respect to testability of a Digital design define controllability and observability .
   (b) Explain the properties of testable digital circuit.
6. Draw the structure of a carry look ahead adder and explain its working principle.
7. Explain about the data - path controller architecture of register transfer machine.
8. Explain clearly about technology dependent logic optimization.

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Code No: RR321202 **Set No.3**

III B.Tech. II Semester Regular Examinations, April/May -2005
VLSI SYSTEMS DESIGN
(Information Technology)

Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
All Questions carry equal marks

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1. Implement the following gates with p-MOS transistors only and explain its working
   (a) 2 Input AND gate.
   (b) 4 Input NOR gate.
2. (a) Why CMOS technology is most suitable for VLSI ICs?
   (b) Compare between CMOS and bipolar technologies.
3. What is a stick diagram and explain about different symbols used for components in stick diagram.
4. Design a layout for CMOS 2- input OR gate.
5. Explain the delay calculation procedure for CMOS inverter.
6. Draw the structure of an un-signed array Multiplier and explain its working.
7. Draw dataflow graphs for the following basic blocks.
   (a) $c \leq a + b;\ d \leq a + x;\ e \leq c + d + x;$
   (b) $W \leq a - b;\ X \leq a + b;\ Y \leq w - x;\ Z \leq y + e;$
   (c) $W \leq a - b;\ X \leq c + w;\ Y \leq x - d;\ Z \leq y + e;$
8. Clearly explain about the generic integrated circuit design flow.

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Code No: RR321202 **Set No.4**

III B.Tech. II Semester Regular Examinations, April/May -2005
VLSI SYSTEMS DESIGN
(Information Technology)

Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
All Questions carry equal marks

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1. Implement the following gates with p-MOS transistors only and explain its working
   (a) 3 Input NAND gate.
   (b) Inverter.
2. Define an integrated circuit and explain clearly different Integrated Circuit design techniques using suitable examples.
3. Design a stick diagram for CMOS two-input NAND and NOR gates.
4. Explain about Pseudo-logic and draw the circuit topology of a three-input NOR gate designed in Pseudo - NMOS.
5. How cross-talk appears in ICs and explain how this cross-talk can be minimized in ICs.
6. Draw the circuit diagram of four transistor DRAM cell with storage nodes and explain its working.
7. Explain clearly block placement phase of the Floor planning of the chip with suitable examples.
8. With suitable example explain any one of the partitioning algorithm

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