Code No: RR321301 **Set No.1**

III B.Tech. II Semester Regular Examinations, April/May -2005
COMPUTER ORGANIZATION
(Electronics & Control Engineering)

Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
All Questions carry equal marks

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1. Explain the expanded structure of the IAS computer with a neat block diagram.
2. (a) Perform the following divide operations.
   (b) Explain how floating point division is done?
      i. 110/111
      ii. 0011/1011
3. (a) Define the elements of a machine instruction
   (b) How various instruction are categorized
   (c) Explain about simple instruction format.
4. (a) List and describe all arithmetic instructions of MIPS R-Series processors
   (b) Discuss how R3000 pipeline can be modified to improve performance
5. (a) Differentiate between unified versus split cache.
   (b) Explain about MESI protocol
   (c) List different Pentium Cache operating modes.
6. (a) Explain about magnetic disk layout
   (b) Elaborate on Winchester disk track format.
7. (a) Differentiate between micro programmed and hard wired control units with merits and demerits of each.
   (b) Discuss about the design considerations of micro instruction sequencing technique.
8. (a) Classify and explain different multiprocessors
   (b) Explain the organization of tightly coupled multiprocessor system with a generic block diagram.

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Code No: RR321301 **Set No.2**

III B.Tech. II Semester Regular Examinations, April/May -2005
COMPUTER ORGANIZATION
(Electronics & Control Engineering)

Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
All Questions carry equal marks

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1. (a) What is instruction Cycle ?
   (b) Elaborate the characteristics of a hypothetical machine
   (c) What do you mean by hardwired program?
2. (a) Find the output binary number after performing the following arithmetic operations
      i. 111.01 + 10.111
      ii. 11.01 + 110.11
      iii. 110.11 - 111.01
   (b) Explain about the longhand division of binary integers.
3. (a) Discuss various aspects of instruction set design.
   (b) Explain about various types of data in detail on which machine instructions operate.
4. (a) Explain about the machine state register.
   (b) Discuss about the sequence of steps that occurs when an interrupt occurs
5. (a) Elaborate on functioning of inverted page table structure.
   (b) Differentiate between ordinary page table and inverted page table
   (c) Why translation-look-aside buffer is used.
6. (a) Elaborate on Intel 8255A programmable peripheral interface with its block diagram and pin layout
   (b) Explain how a keyboard/display can be interfaced to 8255A with a neat diagram
7. (a) Elaborate on control of micro sequencer.
   (b) Discuss about 8832, which is a registered ALU
8. . A pipelined processor has two branch delay slots. An optimizing complier can fill one of these slots 85 percent of the time and can fil second slot only 20 percent of the time. What is the percentage improvement in performance achieved by this optimization?

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Code No: RR321301 **Set No.3**

III B.Tech. II Semester Regular Examinations, April/May -2005
COMPUTER ORGANIZATION
(Electronics & Control Engineering)

Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
All Questions carry equal marks

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1. (a) Draw and explain the instruction cycle state diagram that includes interrupt cycle processing.
   (b) Discuss about transfer of control with multiple interrupts. Demonstrate with a neat diagram
2. (a) Perform the subtraction on the following decimal numbers using 9s complement representation.
      i. 23-12
      ii. 23-29
   (b) A binary computer uses 36 bit registers to store numbers. Eight bits are used for the exponent and the exponent is represented in excess 64 form. Find the approximate range of decimal numbers handled by this computer
3. Explain various characteristics of machine instructions in detail
4. (a) List various R3000 pipeline stages. Also explain the function of each.
   (b) List and describe all shift and multiply/divide instructions of MIPS R-Series processors.
5. (a) What is block hit ratio?
   (b) Explain major variables on which hit ratio depends.
   (c) Discuss about FIFO replacement with two different memory capacities. Give suitable example
6. (a) Differentiate between I/O techniques with and without the use of interrupts.
   (b) Explain different types of I/O commands.
   (c) What is isolated I/O. Differentiate between memory-mapped and isolated I/O with examples.
7. (a) Discuss about the evolution of I/O function.
   (b) Explain the characteristics of I/O channels.
8. (a) Give a summary of arithmetic and logical operations that are defined for the vector architecture.
   (b) What is cache coherence problem. Discuss about different cache coherance approches.

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Code No: RR321301 **Set No.4**

III B.Tech. II Semester Regular Examinations, April/May -2005
COMPUTER ORGANIZATION
(Electronics & Control Engineering)

Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
All Questions carry equal marks

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1. (a) Differentiate between traditional and high performance bus architectures
   (b) List the key elements of bus design.
2. (a) Explain about booth coding
   (b) Find the booth coded numbers of the following binary numbers
      i. 01101111101
      ii. 000111110110
3. (a) Explain about cache management operation of power PC
   (b) List nine separate conditions for conditional branch instructions of power PC.
4. (a) Discuss about RISC pipelining with regular instructions
   (b) How would you optimize RISC pipelining?
   (c) Give reasons for reduction in overall execution rate of RISC processors
5. (a) Explain the principles of segmentation .
   (b) Discuss about address translation in segmentation.
   (c) What is hit ratio?
6. (a) Differentiate between I/O techniques with and without the use of interrupts.
   (b) Explain different types of I/O commands.
   (c) What is isolated I/O. Differentiate between memory-mapped and isolated I/O with examples.
7. (a) List sequencing and branching control fields of IBM 3033 microinstruction.
   (b) Discuss the functioning of micro sequencer with example
8. (a) Discuss about exeception in multiple execution unit pipelined processors with examples.
   (b) Discuss about dispatch and superscalar operation in multiple execution unit pipelined processors

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