Code No: RR321503 **Set No.1**

III B.Tech. II Semester Regular Examinations, January -2005
FAULT TOLERANT SYSTEMS
(Computer Science & Systems Engineering)

Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
All Questions carry equal marks

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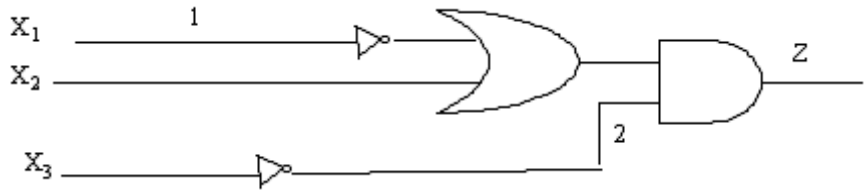
1. (a) What are temporary faults − Explain
   (b) Explain in detail about the Markov model and continuous parameter Morkov model.
   (c) What are the disadvantages of intermittent faults?
2. Using Boolean Difference Methods find the test vectors for SA0 fault on input line 1 and SA1 fault on the internal line 2 of the following circuit using all 6 methods.



3. (a) What is meant by Reliability improvement factor of a system and mission time improvement factor.
   (b) Show that $R_{TMR}^{(t)} = 3R_M^2 - 2\,R_M^3\, where\, R_M$ is the reliability of single modules used in TMR system.
4. (a) With an example explain the practical fault tolerant system?
   (b) How do you enhance the fault tolerance characteristics of digital systems?
5. (a) Design a combinational self − testing checkers for k − out of 2 k codes, which are self-testing.
   (b) List out the importance and advantages of self − checking checker circuits.
6. (a) Explain the general appraoch to the design of totally self-checking PLAs.
   (b) Explain why self-checking machines are essential in digital system.
7. (a) What are the goals of a design for testability?
   (b) What are the different methods available? Explain at least two such techniques.
8. (a) Draw the structure of Built in Self Test for ult under test.
   (b) Explain Exhaustive testing approach for BIST schemes.

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Code No: RR321503 **Set No.2**

III B.Tech. II Semester Regular Examinations, January -2005
FAULT TOLERANT SYSTEMS
(Computer Science & Systems Engineering)

Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
All Questions carry equal marks

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1. (a) Define the terms Reliability, failure rate, maintainability, Availability of a system. How do they help in using the systems upto time T hrs.
   (b) Compare the overall reliability of series to parallel and parallel to series interconnection schemes.
2. Write short notes on
   (a) Random test vector generation
   (b) Transition count testing.
   (c) Compare the above 2 methods with conventional methods.
3. (a) What is the condition with which the Reliability of Triplicated TMR system is greater than basic TMR system.
   (b) Also derive the R(t) function of a Triplicated TMR for a fixed mission time T.
4. (a) What is the mechanism adopted in COPRA a fault Tolerant system. Explain in detail.
   (b) What is meant by Time redundancy? Explain.
5. (a) List out the advantages and disadvantages of self-checking circuit in all aspects.
   (b) Design a totally self-checking checker circuit for a given berger code of length I bits.
6. (a) Explain the advantages of PLA and how it is used as totally self-checking circuit.
   (b) For the given 4 input, 4-output function design a totally self checking checker circuit using PLAs.
   $f_1(A, B, C, D) = \Sigma(0, 2, 3, 7, 8, 10, 12, 13, 15)$
   $f_2(A, B, C, D) = \Sigma(0, 2, 3, 4, 9, 12, 13, 15)$
   $f_3(A, B, C, D) = \Sigma(0, 1, 2, 4, 8, 9, 10, 14)$
   $f_4(A, B, C, D) = \Sigma(0, 1, 2, 4, 5, 6, 8, 11, 14)$.
7. What are the advantages and disadvantages of "Using control logic" technique, Reed Mullars expansion techniques, syndrome testable design and minimally testable network properties?

8. (a) Explain pseudo-exhaustive pattern generation with example.
   (b) Write the concept of autonomous design verification technique.

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Code No: RR321503 **Set No.3**

III B.Tech. II Semester Regular Examinations, January -2005
FAULT TOLERANT SYSTEMS
(Computer Science & Systems Engineering)

Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
All Questions carry equal marks

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1. Derive the reliability function of a parallel, series system compare the results with a fixed R(t) = 0.9 for each module used.
2. (a) A circuit realizes the function.$Z = \overline{X}_1 X_4 + \overline{X}_2 X_3 + X_1\overline{X}_4$. Using Boolean Difference method find the test vectors for SA0, SA1 faults on all input lines of the circuit.
   (b) What are the different properties of Boolean differences? Explain.
3. (a) Explain different fault delection Techniques used in dynamic redundancy system.
   (b) Draw a neat Hybrid (3,s) system and derive the R(t) of this system. Extend the derivation to Hybrid (N,S) system.
4. (a) What is the goal of "pluibus" system used in ARPA network. Explain its working.
   (b) What is ment by fail-soft operation? What should a system have to achieve the capability of fail-soft operation?
5. (a) Explain in detail about a self-checking m out of n code checker.
   (b) Construct a 2 out 7 code checker.
6. Explain in detail about fail-safe sequential circuits design with an example.
7. Write a short notes an
   (a) Controllability
   (b) Observability
   (c) Positive unate function
   (d) Syndrom relations of all types of terminating gates.
8. (a) Discuss the test patterns generated by Liner Feedback Shift Register.
   (b) What is meant by convolved LFSR/SR.

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Code No: RR321503 **Set No.4**

III B.Tech. II Semester Regular Examinations, January -2005
FAULT TOLERANT SYSTEMS
(Computer Science & Systems Engineering)

Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
All Questions carry equal marks

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1. (a) Define reliability and maintainability
   (b) Differentiate the random versus deterministic failure phenomenon.
   (c) What is meant by the reliability function?
2. (a) What are the goals of Design for stability?
   (b) Distinguish between ditermenistic test pattern generation and probabilitstic test pattern generation methods.
3. (a) Explain the 5MR Reconfiguration scheme. Explain in detail the function of each block.
   (b) Discuss the 3 cases for which the 5MR system automatically reconfigure to tolerate single and multiple faults. Explain each with an example.
4. Explain in detain any of the two practical fault Tolerant systems.
5. (a) Write short notes on:
      i. M out n code
      ii. Berger code.
   (b) Explain briefly the coding techniques used in self-checking circuits.
6. (a) Explain the terms τ -partition, η_i^P partition, r_j^P partition used in partition theory to design fail safe synchronary sequential dots.
   (b) When can be say that the sequential circuit is diagnosable? If it is not diagnosable how do you make it diagnosable?
7. (a) Explain three level OR-AND-OR design technique.
   (b) Write a short note on adding control logic in to a combinational logic to have only 5 test pattern.
8. (a) What is meant by circular BIST technique?
   (b) Give a simplified configuration of circular BIST and explain.

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