Code No: RR322203 **Set No.1**

III B.Tech. II Semester Regular Examinations, April/May -2005
MICROPROCESSORS & MICROCONTROLLERS
(Instrumentation & Control Engineering)

Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
All Questions carry equal marks

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1. (a) Give the 8085 compatible flags of 8086 processors? Discuss the design of each flag?
   (b) List out segmentation resisters of 8086? Explain how 8086 provides 1 MB memory address space using the segment registers? What is the purpose of extra segment?
2. (a) Develop a far procedure declared as PUBLIC to convert a 4-digit BCD number to its equivalent hex number?
   (b) Develop a near procedure to find the GCD of two numbers of 2-digit Hex. Use this procedure to find the GCD of three numbers?
3. Describe the function of the following pins in 8086 maximum mode of operation.
   (a) MN/$\overline{MX}$
   (b) $\overline{RQ}/\overline{GT}_0$ $and\overline{RQ}/\overline{GT_1}$
   (c) QS_0 & QS_1
   (d) $\overline{LOCK}$
4. Explain how to interface a stepper motor with 4-step input sequence to 8086 based system with the help of hard ware design? Write the instruction sequence to move the stepper motor 10 steps in clockwise and 12 steps in anti-clockwise direction.
5. (a) Explain demand transfer mode and block transfer mode of 8237?
   (b) Show how 8237's are cascaded to provide more number of DRQ's and explain the operation?
   (c) Explain how memory to memory transfer is performed with 8237?
6. Write an initialization sequence for an 8259 that is the only 8259 in an 8086 based system, with an even address of 0A0H that will cause.
   (a) Request to the level triggered mode
   (b) IR_0 request to an interrupt type 28
   (c) SP/EN to output a disable signal to the data-bus transceivers.
   (d) The ISR bits to be cleared automatically at the end of second INTA pulse.
   (e) The IMR to be cleared.

(f) The highest priority interrupt will be IR_3.

7. A target system based on 8088 processor uses less amount of SRAM. The programs are stored in EPROM that starts from F0000H ends with the address of FFFFFH. The capacity of SRAM is 8KB interfaced at address 00000H. The chip size is 8KB for EPROM and SRAM. Show the complete memory interface?

8. An 8051 based system requires external memory of four 8Kbytes of SRAM each and two chips of EPROM of size 4Kbytes. The EPROM starts at address 1000H. SRAM address map follows EPROM map. Give the complete memory interface?

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1. (a) What is the length of the instruction queue in 8086? Discuss the use of the queue? Explain the reason for limiting the length of queue?
   (b) What is the minimum number of segment resisters that are necessary to provide segmentation? How do access common data for different programs using segmentation?

2. (a) Discuss various branch instruction of 8086 microprocessor, that are useful for relocation?
   (b) Using a do-while construct, develop a sequence of 8086 instructions that reads a character string from the keyboard and after pressing the enter key the character string is to be displayed again.

3. Describe the function of the following pins and their use in 8086 based system.
   (a) DEN
   (b) $\overline{LOCK}$
   (c) $\overline{TEST}$
   (d) READY

4. (a) A DAC is interfaced to 8255 with an address map of 0800H to 0803H. Give the hardware design? It is necessary to design a counter type ADC with the same 8255 and DAC using a comparator. Give the necessary hardware? Provide the necessary instruction sequence to store a sample in location 'sampleone'?
   (b) Using the above hardware write the instruction sequence for successive approximation ADC?

5. (a) Explain demand transfer mode and block transfer mode of 8237?
   (b) Show how 8237's are cascaded to provide more number of DRQ's and explain the operation?
   (c) Explain how memory to memory transfer is performed with 8237?

6. (a) Write an instruction sequence that will cause the priority of an 8259, whose even address is 0800H, to be IR_5, IR_6, IR_7, IR_0, IR_1, IR_2, IR_3, IR_4. Solve this problem when the current priority is IR_1 and for the second time assuming the current priority to be IR_7?
   (b) Explain with examples how interrupt type 1 and type 3 provide debugging feature?

7. (a) With a neat sketch explain the function of memory array of PROM?
   (b) Draw the basic cell structure of EPROM and explain the principle of operation?
   (c) Distinguish between EPROM and E^2PROM? Mention their application areas?

8. Draw and discuss the formats and bit definitions of the following SFR's in 8051 microcontroller?
   (a) PCON
   (b) PSW
   (c) IP
   (d) TMOD

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Code No: RR322203 **Set No.3**

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Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
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1. (a) Compare 8 bit processors and 16 bit processors from the architectural view.
   (b) Explain Overflow condition with 8 bit signed data. Generate Overflow flag using other flags of 8086?
2. Develop an 8086 assembly language program that reads a key from the keyboard and converts it to uppercase before displaying it. The program needs to terminate on typing the 'Enter' key combination.
3. What is function of ready pin in 8086. Draw the circuit diagram for wait state generation between 0 and 7 wait states and draw the corresponding timing diagram.
4. Interface an 8-bit DAC to 8255 with an address map of 0100H to 0103H. The DAC provides output in the range of +5V to 5V. Write the instruction sequence for the following?
   (a) For generating a square wave with a peak to peak voltage of 2V and the frequency will be selected from memory location 'FREQ'.
   (b) For generating a triangular wave with a maximum voltage of +4V and a minimum of 2V.
5. (a) Draw the block diagram of 8251 and explain each block?
   (b) Discuss the serial data transmission standards and their specifications?
6. (a) Write an instruction sequence that when executed will toggle the state of the read resister bit in OCW3. Assume that the 8259 is located at memory address 00A0H.
   (b) How do you set or clear the interrupt flag IF? What is its importance in the interrupt structure of 8086?
   (c) How 8259 can be programmed for rotating interrupt request priorities. Explain?
7. (a) With a neat sketch explain the function of memory array of PROM?
   (b) Draw the basic cell structure of EPROM and explain the principle of operation?
   (c) Distinguish between EPROM and E^2PROM? Mention their application areas?
8. Discuss the following signal descriptions?

(a) ALE/PROG
(b) $\overline{EA}/V_{PP}$
(c) $\overline{PSEN}$
(d) RXD
(e) $\overline{INT_o}$ / $\overline{INT_1}$
(f) TXD
(g) T_0 AND T_1
(h) $\overline{RD}$

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Code No: RR322203 **Set No.4**

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Time: 3 hours **Max Marks: 80**

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1. (a) Give the 8085 compatible flags of 8086 processors? Discuss the design of each flag?
   (b) List out segmentation resisters of 8086? Explain how 8086 provides 1 MB memory address space using the segment registers? What is the purpose of extra segment?
2. (a) What are the different ways of passing parameters to and from procedures? Explain the methods with examples in assembly language?
   (b) Give a neat flow chart and the corresponding 8086 assembly language program for performing bubble sort in an array of N elements of 4-digit Hex numbers.
3. (a) What is the purpose of ALE, BHE, DT/$\overline{R}$ and $\overline{DEN}$ pins of 8086? Show their timing in the system bus cycle of 8086?
   (b) Show the complete design to generate system address, data and control buses using the above pins, latches and transceivers.
4. (a) What is BSR mode operation? How it is useful in controlling the interrupt initiated data transfer for mode 1 and 2?
   (b) Explain the transistor buffer circuit used to drive 7-segment LEDs?
5. (a) How do we connect RS-232C equipment
      i. To data terminal type devices?
      ii. To serial port of SDK 86, RS-232C connection?
   (b) Give the specifications of RS-232C.
6. With detailed hardware and the associated algorithm, explain how a real time clock will be implemented in an 8086 based system.
7. In an SDK-86 kit 64KB SRAM and 32KB EPROM is provided on system and provision for expansion of another 64KB SRAM is given. The on system SRAM address map is from 00000H to 0FFFFH and that of EPROM is from F8000H to FFFFFH. The expansion slot address map is from 80000H to 8FFFFH. The size of SRAM chip is 32KB. EPROM chip size is 16KB. Give the complete memory interface and also the address map for individual chips?
8. Draw and discuss the formats and bit definitions of the following SFR's in 8051 microcontroller?

(a) PSW
(b) IE
(c) SCON
(d) TMOD

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