Code No: NR411905 **NR**

IV B.Tech I Semester Supplementary Examinations, April/May 2005
VLSI TECHNOLOGY
(Electronics & Computer Engineering)

Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
All Questions carry equal marks

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1. (a) Explain in detail the p-well process for CMOS fabrication indicating the masks used.
   (b) Draw a neat sketch of CMOS inverter fabricated using n-well process.
2. (a) What are lambda based design rules? High light their merits and demerits.
   (b) Draw the following wires with appropriate colour / monochrome code using lambda based design rules:
      i. n diffusion
      ii. Polysilicon
      iii. Metal-1
      iv. Metal 2
3. (a) What are the advantages of PLAs
   (b) Give the sketch for AND matrix used in PLAs and explain its functionality
4. (a) With the help of a block diagram explain the working of FPGA
   (b) What are the differences in design approach in the case of ASIC design and semi custom Design
5. (a) Explain about Automatic test vector generation.
   (b) How fault simulation is done and explain fault models with the help of examples.
6. (a) Explain how a physical fault is translated to Logical fault.
   (b) Describe the structure at fault model.
7. (a) How packaging is affects on the performance of VLSI chip?
   (b) Explain surface mounting type packages.
8. (a) What are the key aspects of switch capacitor?
   (b) What are the different methods to design switched capacitor filters in VLSI.

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