Code No: NR210203 **NR**

II B.Tech I Semester Supplementary Examinations, November 2005
SWITCHING THEORY & LOGIC DESIGN
(Common to Electrical & Electronic Engineering, Electronics & Communication Engineering, Computer Science & Engineering, Electronics & Instrumentation Engineering, Information Technology, Electronics & Control Engineering, Computer Science & Systems Engineering, Electronics & Telematics and Electronics & Computer Engineering)

Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
All Questions carry equal marks

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1. (a) Show the weights of three different four bit Self-Complementing codes whose only negative weight is -4.
   (b) Encode each of the ten decimal digits 0,1,.....9 by means of the weighted binary codes obtained in (a).

   [6+10]

2. (a) Find the minimal expression for the function f(w,x,y,z)=$\sum$(0,2,5,9,15) +$\sum$d (6,7,8,10,12,13) using Karnaughs-map.
   (b) i. Determine the Canonical sum-of-products form for $T(x, y, z) = \overline{x}y + \overline{z} + xyz$
   ii. Minimize the function $f(x, y, z, w) = x + xyz + wx + \overline{x}y + \overline{w}x + \overline{x}yz$.

   [8+4+4]

3. (a) Implement the following function using only NOR gates F=a .(b+ c.d) + (b . $\overline{c}$).
   (b) Implement the following function using only NAND gates G=(a + $\overline{b}$). (c. d + $\overline{e}$)
   (c) Give the minimum two-level SOP realization of the following switching function using only NAND gates. F(x,y,z) = $\sum$ m (0,3,4,5,7)

   [4+4+8]

4. (a) Implement the following function using a multiplexer of proper size. F(w,x,y,z) = $\sum m(0, 1, 2, 3, 4, 9, 13, 14, 15)$
   (b) Draw the circuit diagram of a 4 bit look a head carry generator circuit.

   [8+8]

5. (a) Draw and explain with the help of truth table the logic diagram of a master slave D flip-flop using NAND gates. With active low preset and clear and with negative edge triggered clock.
   (b) Give the transition table for RS flip flop.

(c) Convert JK flip flop into T and D flip flops.

[8+2+6]

6. (a) Draw the state diagram for the synchronous sequential circuit with inputs (x_1, x_2) and single output z in which the input pair represents alphabet letters as given below.

A-00
B-01
C-10
D-11

The output is 1 if the most recent two inputs are in alphabetic order (i.e.) AB, BC and CD.

(b) Draw the circuit diagram of R-S flip flop with active low preset and clear with level mode clock. What is the disadvantage in using level mode clock? How to overcome this problem. Discuss.

[8+8]

7. For the machine shown in the table below obtain:

(a) The corresponding reduced machine table in standard form

(b) Find a minimum length that distinguishes state A from state B where PS: present state, NS: next state, Z: output, X: input

PS	NS,Z	
	X=0	X=1
A	B,1	H,1
B	F,1	D,1
C	D,0	E,1
D	C,0	F,1
E	D,1	C,1
F	C,1	C,1
G	C,1	D,1
H	C,0	A,1

[10+6]

8. Obtain the ASM charts for the following state transition

(a) If x = 0, control goes from T1 to state T2, if x = 1, generate the conditional operation and go from T1 to T2.

(b) If x = 1, control goes from T1 to T2 and then to T3, if x = 0, control goes from T1 to T3.

(c) Start from state T1, then if xy = 00, go to T2, if xy = 01, then go to T3, if xy = 10, then go to T1, otherwise go to T3. and design its control circuit using

i. D flip flop & decoder

ii. Input multiplexer & a register

[8+8]

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