Code No: RR210202 **Set No. 1**

II B.Tech I Semester Regular Examinations, November 2005
PULSE AND DIGITAL CIRCUITS
(Common to Electrical & Electronic Engineering, Electronics & Communication Engineering, Electronics & Telematics and Electronics & Computer Engineering)

Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
All Questions carry equal marks

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1. A current pulse of amplitude I is applied to a parallel RC combination. Plot to scale the waveforms of the current i_C for the cases
   (a) $t_p < R_C$,
   (b) t_p=RC
   (c) $t_p >$ RC where t_p is the pulse width.(figure1)

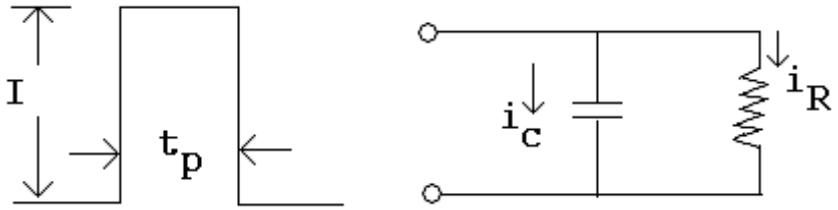

Figure 1:

[6+5+5]

2. (a) Draw the circuit diagram of slicer circuit using Zener diodes and explain its operation with the help of its transfer characteristic. [6]
   (b) For the circuit shown in figure 2 below:

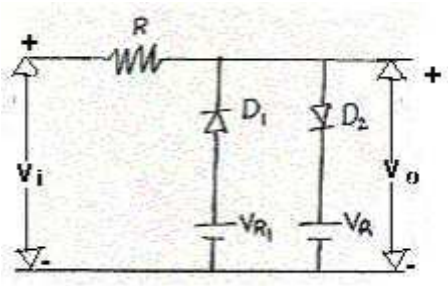

Figure 2:

If R = 1KΩ, V_{R2} = 10V, V_{R1} = 7 V
R_f = 0 and $R_r = \propto$

   i. Sketch the transfer characteristic

ii. If $V_i = 20 \sin \omega t$ sketch the input and output waveforms. [10]

3. (a) Explain the phenomenon of "latching" in a transistor switch. [6]

   (b) A transistor has f_T = 50 MHz, h_{FE}=40, $C_{b'c}$=3PF and operates with V_{cc}=12 V and R_c=500 Ω. The transistor is operating initially in the neighbourhood of the cut-in point. What base current must be applied to drive the transistor to saturation in 1μ sec? [10]

4. (a) Draw the circuit diagram of self-bias with symmetrical triggering using diodes. Explain the working of the same. [8]

   (b) Compare between triggering at base and collectors. [8]

5. With reference to voltage sweeps explain the following terms: [16]

   (a) Sweep speed

   (b) Linearity of sweep

   (c) Sweep stability

   (d) Recovery time.

6. (a) Explain the operation of a sweep circuit as a divider. [8]

   (b) The UJT relaxation oscillator is to be used as a 3:1 divider for pulses which occur at a 2500 Hz rate. The available supply voltage is 30 V. The pulses are applied at base B_2. Draw the circuit and calculate pulse amplitude. [8]

7. (a) Illustrate with neat circuit diagram, the operation of unidirectional sampling gate for multiple inputs. [8]

   (b) Explain with circuit diagram the operation of a two input sampling gate which does not have any loading effect on control signal. [8]

8. (a) Explain the triggering arrangement for blocking oscillator. [8]

   (b) Discuss the effect of switching due to magnetic saturation. Show the hysteresis and current waveforms. [8]

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Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
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1. (a) Prove that an RC circuit behaves as a reasonably good integrator if RC>>15T, where T is the period of an input 'E_m Sin wt'. [10]
   (b) What is the ratio of the rise time of the three sections in cascade to the rise time of a single section of low pass RC circuit. [6]

2. (a) What is meant by clipping in wave shaping? [4]
   (b) Classify different types of clipper circuits. Give their circuits and explain their operation with the aid of transfer characteristics. [12]

3. (a) Explain the phenomenon of "latching" in a transistor switch. [6]
   (b) A transistor has f_T = 50 MHz, h_{FE}=40, $C_{b'c}$=3PF and operates with V_{cc}=12 V and R_c=500 Ω. The transistor is operating initially in the neighbourhood of the cut-in point. What base current must be applied to drive the transistor to saturation in 1μ sec? [10]

4. For the Schmitt trigger circuit (figure 1) shown below, find UTP &LTP. Derive the formula used. For an input vi=15 sin ωt, plot the output waveform. Data given are: [16]

   V_{cc}=15v, Rs=3k, Rc1=3k, Rc2=1k, R1=4k, R2=15k, & Re=6kΩ.

5. (a) Bring out the necessity and importance of current sweep circuits. List out its applications. [8]
   (b) What are the techniques used to improve the linearity of current sweeps. Illustrate with examples. [8]

6. (a) Explain how a sinusoidal oscillator can be used as a frequency divider. [8]
   (b) Write short notes on
      i. Phase delay and
      ii. Phase jitters [8]

7. (a) Explain the operation of unidirectional diode sampling gate with neat sketch of waveforms. Illustrate the effect of different levels of control voltage on gate output. [10]
   (b) Discuss the advantages and disadvantages. [6]

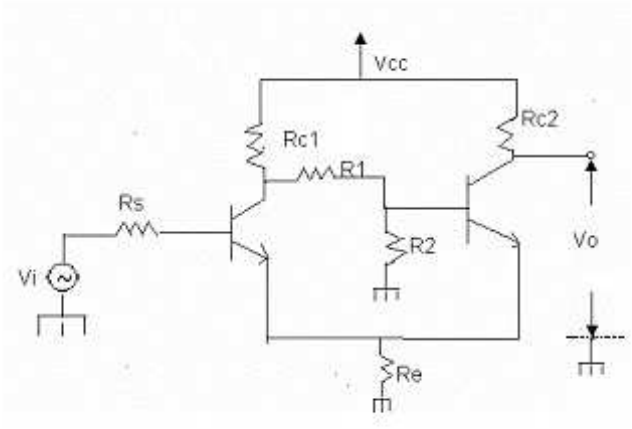

Figure 1:

8. (a) Compare the diode controlled and RC controlled astable operated blocking oscillator. [6]
   (b) What are the advantages of RC controlled oscillator? [4]
   (c) List the applications of blocking oscillators. [6]

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Code No: RR210202 **Set No. 3**

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Answer any FIVE Questions
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1. (a) Three low pass RC circuits are in cascade and isolated from one another by ideal buffer amplifiers. Find the expression for the output voltage as a function of time if the input is a step voltage. [10]
   (b) Find the rise time of the output in terms of RC in the above case. [6]

2. (a) Draw the basic circuit diagram of negative peak clamper circuit and explain its operation. [6]
   (b) For the circuit shown in figure 1 below, an input voltage V_i linearly varies from 0 to 150 V is applied. Sketch the output voltage V_0 to the same time scale. [10]
   Assume ideal diodes.

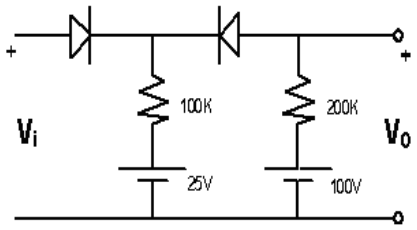

Figure 1:

3. (a) Explain the behavior of a BJT as a switch. Give Applications. [8]
   (b) Write a short note on switching times of a transistor. [8]

4. (a) Explain how a Schmitt trigger can be used as a comparator and as a squaring circuit. [8]
   (b) What do you understand by hysterisis? What is hysterisis voltage? Explain how hystersis can be eliminated in a Schmitt trigger. [8]

5. (a) Draw the circuit of a two-stage transistor bootstrap circuit to get an exactly linear sweep. [8]
   (b) Draw a practical form of a bootstrap sweep circuit using a transistor. Write the expressions for sweep speed and linearity of such circuit. [8]

6. (a) How astable multivibrator can be synchronized? Illustrate with waveforms.[8]

(b) A symmetrical astable multivibrator using transistor operates from 10V supply has a period of 1msec. Triggering pulses of spacing 750 microsec are applied to one base through a small capacitor from a high-impedance source. Find the minimum triggering pulse amplitude required to achieve 1:1 synchronization. [8]

7. (a) What is a sampling gate? Explain the operation of series gate using JFET. Sketch the input and output waveforms. [8]

   (b) Illustrate the errors encountered in series sampling and what is the design procedure to minimize these errors? [8]

8. In an astable transistor (diode controlled) blocking oscillator, if L = 5.2 mH, C = 90 pF, V_{CC}= = 10 V, R = 500 Ω, V_r = 6V, η = 1 and V_{BB} = 0.5V. Calculate

   (a) the period and duty cycle of free oscillations [6]

   (b) the peak voltage and currents [4]

   (c) the current in the magnetizing inductance at the end one cycle. [6]

   Neglect saturation junction voltages.

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1. (a) Verify $V_1 = \frac{V}{1+e^{-T/2RC}}$ $V_1' = \frac{V}{1+e^{T/2RC}}$ (figure1)

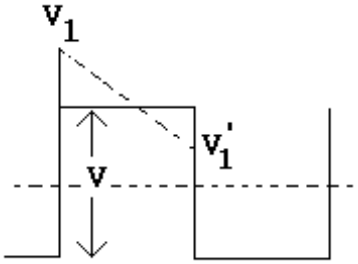

Figure 1:

For a symmetrical square wave applied to a high pass RC circuit. [10]

(b) Draw the RC high pass circuit and explain its working with step voltage input. [6]

2. (a) State and prove clamping-circuit theorem. [6]

(b) A square wave input as shown in figure 2 below is applied to the clamping circuit. Sketch the steady-state output waveform and derive the necessary expressions. [10]

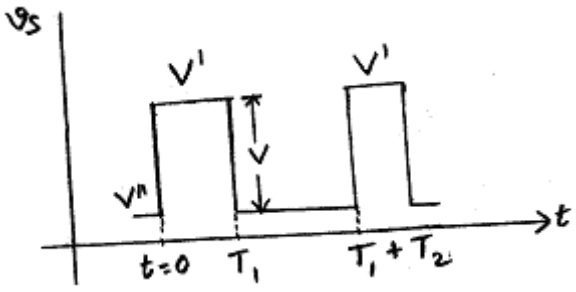

Figure 2:

3. (a) Explain the behavior of a BJT as a switch. Give Applications. [8]

(b) Write a short note on switching times of a transistor. [8]

4. The binary circuit (figure 3) given below uses silicon transistors with h_{FE}=20. Calculate V_1 and V_2, for a sine wave input Vi=10 Sin wt. Plot V_{CN1}, V_{EN}, V_{CN2} as a function of α=wt. (V_1 is the input voltage when Q_1 begins conducting and V_2 is the input voltage when Q_2 resumes conducting.) [16]

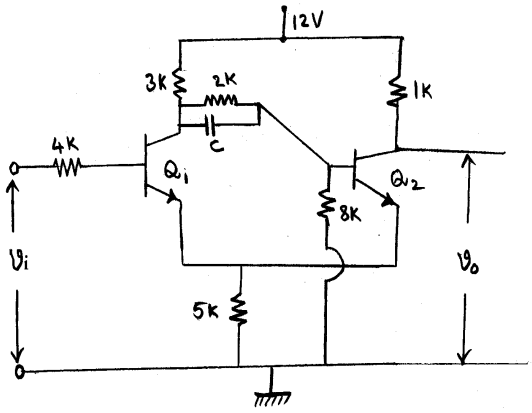

Figure 3:

5. (a) Draw the circuit of a constant current sweep circuit and derive the expression for sweep voltage. [8]
   (b) In transistor constant current sweep circuit what happens if temperature is increased? What sort of circuit provides temperature compensation? [8]

6. (a) Illustrate the terms 'synchronization' and 'frequency division' of a sweep generator. [8]
   (b) A free-running relaxation oscillator has sweep amplitude of 100 V and a period of 1 msec synchronizing pulses are applied to the device such that breakdown voltage is lowered by 50 V at each pulse. The synchronizing pulse frequency is 4 kHz. What is the amplitude and frequency of synchronized oscillator waveform? [8]

7. (a) What is a sampling gate? Explain the operation of series gate using JFET. Sketch the input and output waveforms. [8]
   (b) Illustrate the errors encountered in series sampling and what is the design procedure to minimize these errors? [8]

8. Explain with neat circuit diagram of triggered blocking oscillator with emitter timing. Draw the equivalent circuit and show the current and voltage waveforms. Derive an expression for current pulse width. [16]

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