Code No: RR210203 **Set No.1**

II B.Tech. I Semester Regular Examinations, November -2005
SWITCHING THEORY AND LOGIC DESIGN
(Common to Electrical & Electronic Engineering, Electronics & Communication Engineering, Computer Science & Engineering, Electronics & Instrumentation Engineering, Bio-Medical Engineering, Information Technology, Electronics & Control Engineering, Computer Science & Systems Engineering, Electronics & Telematics and Electronics & Computer Engineering)

Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
All Questions carry equal marks

⋆ ⋆ ⋆ ⋆ ⋆

1. (a) Perform the subtraction with the following unsigned binary numbers by taking the 2's complement of the subtrahend.
   i. 11010-10000
   ii. 11010-1101
   iii. 100-110000
   iv. 1010100-1010100
   (b) The binary numbers listed have a sign bit in the left most position and, if negative, are in 1's complement form. Perform the arithmetic operations indicated and verify the answers.
   i. 101011+111000
   ii. 001110+110010
   iii. 111001-001010
   iv. 101011-100110

   [8+8]

2. (a) Simplify the function using Karnaugh map method F (A,B,C,D) = $\sum$(4,5,7,12,14,15)+ $\sum$d(3,8,10).
   (b) Give three possible ways to express the function F = $\overline{A}\ \overline{B}\ \overline{D} + \overline{A}\ \overline{B}\ \overline{C}\ \overline{D} + \overline{A}BD + AB\overline{C}D$ with eight or less literals.

   [8+8]

3. (a) Implement the following function using only NOR gates F=a .(b+ c.d) + (b . $\overline{c}$).
   (b) Implement the following function using only NAND gates G=(a + $\overline{b}$). (c. d + $\overline{e}$)
   (c) Give the minimum two-level SOP realization of the following switching function using only NAND gates. F(x,y,z) = $\sum$ m (0,3,4,5,7)

   [4+4+8]

4. Implement the following functions using a PROM

(a) F(w,x,y,z) = $\sum$(1,9,12,15)

(b) G(w,x,y,z)= $\sum$ (0,1,2,3,4,5,7,8,10,11,12,13,14,15)

[8+8]

5. (a) Convert the following

   i. J-K-flip-flop to T-flip-flop

   ii. R-S flip-flip to D-flip-flop

   (b) Draw the schematic circuit of R-S master-slave Flip-Flop. Give its truth-table and justify the entries in the truth-table.

[8+8]

6. (a) Draw the state diagram for the synchronous sequential circuit with inputs (x_1, x_2) and single output z in which the input pair represents alphabet letters as given below.

   A-00
   B-01
   C-10
   D-11

   The output is 1 if the most recent two inputs are in alphabetic order (i.e.) AB, BC and CD.

   (b) Draw the circuit diagram of R-S flip flop with active low preset and clear with level mode clock. What is the disadvantage in using level mode clock? How to overcome this problem. Discuss.

[8+8]

7. Find the equivalence partition for the given machine. Show a standard form of the corresponding reduced machine.

PS	NS,Z	
	X=0	X=1
A	F,0	B,1
B	G,0	A,1
C	B,0	C,1
D	C,0	B,1
E	D,0	A,1
F	E,1	F,1
G	E,1	G,1

[16]

8. Obtain the ASM charts for the following state transition

   (a) If x = 0, control goes from T1 to state T2, if x = 1, generate the conditional operation and go from T1 to T2.

(b) If x = 1, control goes from T1 to T2 and then to T3, if x = 0, control goes from T1 to T3.

(c) Start from state T1, then if xy = 00, go to T2, if xy = 01, then go to T3, if xy = 10, then go to T1, otherwise go to T3. and design its control circuit using

i. D flip flop & decoder

ii. Input multiplexer & a register

[8+8]

⋆ ⋆ ⋆ ⋆ ⋆

Code No: RR210203 **Set No.2**

II B.Tech. I Semester Regular Examinations, November -2005
SWITCHING THEORY AND LOGIC DESIGN
(Common to Electrical & Electronic Engineering, Electronics & Communication Engineering, Computer Science & Engineering, Electronics & Instrumentation Engineering, Bio-Medical Engineering, Information Technology, Electronics & Control Engineering, Computer Science & Systems Engineering, Electronics & Telematics and Electronics & Computer Engineering)

Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
All Questions carry equal marks

⋆ ⋆ ⋆ ⋆ ⋆

1. (a) Perform the subtraction with the following unsigned binary numbers by taking the 2's complement of the subtrahend.
   i. 11010-10000
   ii. 11010-1101
   iii. 100-110000
   iv. 1010100-1010100
   (b) The binary numbers listed have a sign bit in the left most position and, if negative, are in 1's complement form. Perform the arithmetic operations indicated and verify the answers.
   i. 101011+111000
   ii. 001110+110010
   iii. 111001-001010
   iv. 101011-100110

   [8+8]

2. (a) Obtain the simplified expression in sum of products for the following Boolean functions using Karnaugh-Map.
   i. F(w,x,y,z) =$\sum$ (1,3,7,11,15) + $\sum_d$ (0, 2, 5)
   ii. F(A, B,C,D) = ABD+ $\overline{A}$ $\overline{C}$ $\overline{D}$+ $\overline{A}$ B+ $\overline{A}$ C $\overline{D}$+A $\overline{B}$ D
   (b) Show the truth table for each of the following function and find its simplest product of sums form.(POS)
   i. $f(x, y, z) = xy + xz$
   ii. $f(x, y, z) = \overline{x} + y\overline{z}$

   [8+8]

3. Implement the function F with the following two level forms
   (a) NAND-AND,
   (b) AND-NOR,

(c) OR-NAND and

(d) NOR-OR
$F(A, B, C, D) = \sum(0,1,2,3,4,8,9,12)$

[16]

4. (a) Write a note on 'high-speed adders'

(b) Give the logic realization of a two bit word comporator to compare two words A=A_1 A_0 and $B = B_1$ B_0 in binary code.

(c) Implement the following function using eight to-one mux F(x, y, z) = $\sum m(0, 2, 3, 5)$

[4+8+4]

5. (a) Define the following terms in connection with a flip-flop

i. set-up time
ii. hold-time
iii. propagation delay time
iv. preset
v. clear

(b) Draw the schematic circuit of D-Flip-Flop with negative edge triggering using NAND gates. Give its truth-table and explain its operation

[10+6]

6. (a) Draw the state diagram for the synchronous sequential circuit with inputs (x_1, x_2) and single output z in which the input pair represents alphabet letters as given below.

A-00
B-01
C-10
D-11

The output is 1 if the most recent two inputs are in alphabetic order (i.e.) AB, BC and CD.

(b) Draw the circuit diagram of R-S flip flop with active low preset and clear with level mode clock. What is the disadvantage in using level mode clock? How to overcome this problem. Discuss.

[8+8]

7. For the machine shown in the table below obtain:

(a) The corresponding reduced machine table in standard form

(b) Find a minimum length that distinguishes state A from state B where PS: present state, NS: next state, Z: output, X: input

PS	NS,Z	
	X=0	X=1
A	B,1	H,1
B	F,1	D,1
C	D,0	E,1
D	C,0	F,1
E	D,1	C,1
F	C,1	C,1
G	C,1	D,1
H	C,0	A,1

[10+6]

8. Obtain the ASM charts for the following state transition

(a) If x = 0, control goes from T1 to state T2, if x = 1, generate the conditional operation and go from T1 to T2.

(b) If x = 1, control goes from T1 to T2 and then to T3, if x = 0, control goes from T1 to T3.

(c) Start from state T1, then if xy = 00, go to T2, if xy = 01, then go to T3, if xy = 10, then go to T1, otherwise go to T3. and design its control circuit using

i. D flip flop & decoder

ii. Input multiplexer & a register

[16]

⋆ ⋆ ⋆ ⋆ ⋆

Code No: RR210203 **Set No.3**

II B.Tech. I Semester Regular Examinations, November -2005
SWITCHING THEORY AND LOGIC DESIGN
(Common to Electrical & Electronic Engineering, Electronics & Communication Engineering, Computer Science & Engineering, Electronics & Instrumentation Engineering, Bio-Medical Engineering, Information Technology, Electronics & Control Engineering, Computer Science & Systems Engineering, Electronics & Telematics and Electronics & Computer Engineering)

Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
All Questions carry equal marks

⋆ ⋆ ⋆ ⋆ ⋆

1. (a) Given the 8bit data word01011011, generate the 12 bit composite word for the Hamming code that corrects and detects single errors.
   (b) A 12 bit Hamming code word containing 8 bits of data and 4 parity bits is read from memory. What was the original 8 bit word if the 12 bit read out is as follows.
      i. 0000 1110 1010
      ii. 1011 1000 0110
      iii. 1011 1111 0100

   [10+6]

2. (a) Minimise the following expression using Karnaugh -map
   f (A,B,C,D) =$\sum$m (1,4,7,10, 13) +$\sum$d (5,14,15)
   (b) Find the complement and dual of the function below and then reduce it to a minimum number of literals in each case. f = [($\overline{ab}$)a][($\overline{ab}$)b].

   [8+8]

3. (a) Derive Boolean expression for a 2input Ex-OR gate to realize with 2 input NAND gates without using complemented variables and draw the circuit.
   (b) Redraw the given circuit in (figure1)after simplification .

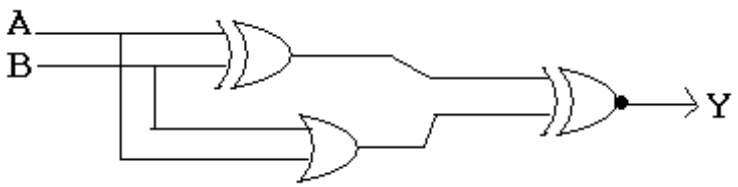

Figure 1:

[8+8]

4. Design a PLA to realize the following three logic functions and show the internal connections
   $F_1(a,b,c,d,e) = \overline{a}\overline{b}\ \overline{d} + \overline{b}c\overline{d} + \overline{a}bcd\overline{e}$
   $F_2(a,b,c,d,e) = \overline{a}be + \overline{b}c\overline{d}e$
   $F_3(a,b,c,d,e) = \overline{a}\overline{b}\ \overline{d} + \overline{b}c\overline{d}e + \overline{a}bcd$ [16]

5. (a) Distinguish between combinational logic and sequential logic
   (b) Draw the schematic circuit of an edge triggered J-K - Flip-Flop with "active low preset" and "active low clear" using NAND gates and explain its operations with the help of Truth-Table.

   [6+10]

6. Derive the state diagram and state table for two input(x_1, x_2) and single output z asynchronous circuit. The output of the circuit $z = x_1$ if $x_2 = 1$, but if $x_2 = 0$, the output is to remain fixed at its last value before x_2 becomes zero and design the circuit using D-flip flops. [16]

7. For the machine given below, find the equivalence partition and a corresponding reduced machine in standard form and also explain the procedure:

PS	NS,Z	
	X=0	X=1
A	B,0	E,0
B	E,0	D,0
C	D,1	A,0
D	C,1	E,0
E	B,0	D,0

   [16]

8. (a) Explain in detail the block diagram of ASM chart.
   (b) Draw the portion of an ASM chart that specifies the conditional operation to increment register R during state T1 and transfer to state T2, if control inputs z and y are = 1 and 0 respectively.

   [8+8]

⋆ ⋆ ⋆ ⋆ ⋆

Code No: RR210203 **Set No.4**

II B.Tech. I Semester Regular Examinations, November -2005
SWITCHING THEORY AND LOGIC DESIGN
(Common to Electrical & Electronic Engineering, Electronics & Communication Engineering, Computer Science & Engineering, Electronics & Instrumentation Engineering, Bio-Medical Engineering, Information Technology, Electronics & Control Engineering, Computer Science & Systems Engineering, Electronics & Telematics and Electronics & Computer Engineering)

Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
All Questions carry equal marks

⋆ ⋆ ⋆ ⋆ ⋆

1. (a) A person on SATURN possessing 18 fingers has a property worth (1,00,000)18. He has 3 daughters and two sons. He wants to distribute half the money equally to his sons and the remaining half to his daughters equally. How much his each son and each daughter will get in Indian currency?
   (b) An Indian started on an expedition to SATURN with Rs.1,00,000. The expenditure on SATURN will be in the ratio of 1:2:7 for food, clothing and traveling. How much he will be spending on each item in the currency of SATURN.

   [8+8]

2. (a) Simplify the function using Karnaugh map method F (A,B,C,D) = $\sum$(4,5,7,12,14,15)+ $\sum$d(3,8,10).
   (b) Give three possible ways to express the function F = $\overline{A}\ \overline{B}\ \overline{D} + \overline{A}\ \overline{B}\ \overline{C}\ \overline{D} + \overline{A}BD + AB\overline{C}D$ with eight or less literals.

   [8+8]

3. Implement the function F with the following two level forms
   (a) NAND-AND,
   (b) AND-NOR,
   (c) OR-NAND and
   (d) NOR-OR
   $F(A, B, C, D) = \sum$(0,1,2,3,4,8,9,12)

   [16]

4. (a) Write a note on 'high-speed adders'
   (b) Give the logic realization of a two bit word comporator to compare two words A=$A_1\ A_0$ and $B = B_1\ B_0$ in binary code.
   (c) Implement the following function using eight to-one mux F(x, y, z) = $\sum m(0, 2, 3, 5)$

   [4+8+4]

5. (a) Explain the following terms in connection with a flip-flop
   i. flip-flop
   ii. race condition
   iii. race around conductions
   (b) Draw the schematic circuit of S-R Flip-Flop with negative edge triggering and give its Truth-Table. Justify the entries in the Truth-Table.

[6+10]

6. (a) Draw the circuit diagram of 4-bit ring counter using D-flip flops and explain its operation with the help of bit pattern.
   (b) Draw the circuit diagram of 4-bit Johnson counter using D-flip flop and explain its operation with the help of bit pattern.

[8+8]

7. For the machine shown in the table below obtain:
   (a) The corresponding reduced machine table in standard form
   (b) Find a minimum length that distinguishes state A from state B where PS: present state, NS: next state, Z: output, X: input

PS	NS,Z	
	X=0	X=1
A	B,1	H,1
B	F,1	D,1
C	D,0	E,1
D	C,0	F,1
E	D,1	C,1
F	C,1	C,1
G	C,1	D,1
H	C,0	A,1

[10+6]

8. Obtain the ASM charts for the following state transition
   (a) If x = 0, control goes from T1 to state T2, if x = 1, generate the conditional operation and go from T1 to T2.
   (b) If x = 1, control goes from T1 to T2 and then to T3, if x = 0, control goes from T1 to T3.
   (c) Start from state T1, then if xy = 00, go to T2, if xy = 01, then go to T3, if xy = 10, then go to T1, otherwise go to T3. and design its control circuit using
      i. D flip flop & decoder
      ii. Input multiplexer & a register

[16]

⋆ ⋆ ⋆ ⋆ ⋆