

II B.Tech I Semester Supplementary Examinations, November 2005
PULSE & DIGITAL CIRCUITS
 (Common to Electrical & Electronic Engineering, Electronics &
 Communication Engineering, Electronics & Telematics and Electronics &
 Computer Engineering)

Time: 3 hours

Max Marks: 80

Answer any FIVE Questions
All Questions carry equal marks

1. (a) Three low pass RC circuits are in cascade and isolated from one another by ideal buffer amplifiers. Find the expression for the output voltage as a function of time if the input is a step voltage. [10]
- (b) Find the rise time of the output in terms of RC in the above case. [6]
2. (a) Design a clipping circuit with ideal components, which can give the waveform shown in figure 1 below for a sinusoidal input. [8]

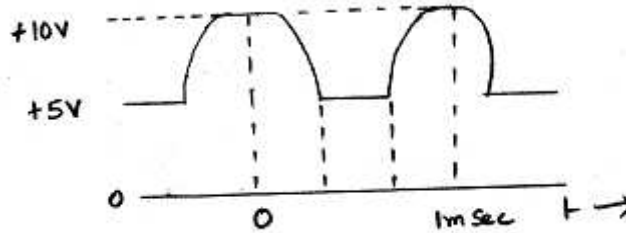


Figure 1:

- (b) Design a diode clamper to restore a d.c level of +3 Volts to an input signal of peak to peak value of 10 Volts. Assume drop across diode is 0.6 Volts. as shown in the figure (figure 2) below [8]

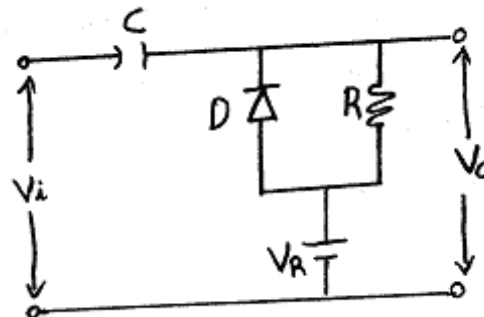


Figure 2:

3. (a) Explain in detail the junction diode switching times. [8]
- (b) Give a brief note on piece-wise linear diode characteristics. [8]

4. (a) What is a direct connected binary circuit? Explain the direct connected binary with the help of a circuit diagram. [8]
(b) Mention the advantages and disadvantages of the above. Mention its use. [8]
5. (a) Distinguish between voltage and current time base generators. [6]
(b) In the current-sweep circuit, how linearity can be corrected through adjustment of driving waveform. Illustrate with an example. [10]
6. (a) Explain how a sinusoidal oscillator can be used as a frequency divider. [8]
(b) Write short notes on
 - i. Phase delay and
 - ii. Phase jitters[8]
7. (a) What is a sampling gate? Explain the operation of series gate using JFET. Sketch the input and output waveforms. [8]
(b) Illustrate the errors encountered in series sampling and what is the design procedure to minimize these errors? [8]
8. (a) Discuss the methods of controlling output current pulse width in blocking oscillators. [6]
(b) Write notes on hysteresis effect in blocking oscillators. [4]
(c) Discuss the method of improving rise time in blocking oscillator. [6]

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