Code No: RR221401 **Set No. 1**

II B.Tech II Semester Supplementary Examinations, November/December 2005
ELECTRONIC DEVICES AND CIRCUITS
(Mechatronics)

Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
All Questions carry equal marks

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1. (a) Derive the expression for the barrier potential Vo at the junction of a P-N diode
   (b) Explain the situation for the occurrence of the phenomenon of Avalanche breakdown in semiconductor diodes and discuss the consequences.
   (c) Draw the equivalent circuit of a Semiconductor diode and briefly explain, how the diode acts as a switch. [6+5+5]

2. (a) Draw the voltage current characteristic of Tunnel Diode.
   (b) Discuss the practical utility of various regions on the Tunnel Diode Characteristic.
   (c) Discuss the favourable conditions for Tunneling Phenomena in Tunnel Diodes.
   (d) Discuss the factors responsible for using Tunnel Diode in high frequency applications. [4x4]

3. (a) Draw a diagram showing the input and output diode representation of a NPN Transistor with biasing voltages so that the Transistor can be operated as an amplifying device.
   (b) Discuss qualitatively the conditions of flow of currents through a NPN Transistor contributing to the fact that Emitter current is the sum of Collector and Base currents
   (c) Define the parameter Emitter injection efficiency and discuss its significance
   (d) If the Emitter current I_E =10ma and Collector Current I_C = 9.5 ma in a Transistor device, calculate the parameters β_{DC} and α_{DC} of the Transistor. [4x4]

4. (a) Draw the circuit diagrams showing the three configurations of Transistor amplifiers.
   (b) Draw the Transistor biasing circuit using Collector-to-base bias arrangement. Explain the concept of providing proper bias for the Transistor to act as amplifying device
   (c) Mention the DC load line equation for CE Transistor Collector to base bias circuit and describe the method of drawing the DC load line on the CE Transistor output characteristics. [6+6+4]

5. (a) Discuss the four basic methods of coupling for cascading of amplifiers to obtain Multi-Stage amplifiers and mention the reasons for cascading of amplifiers.
   (b) Draw a typical block diagram of 3-stage CE Cascaded amplifier.
   (c) Derive the expressions for voltage gain and the resultant phase shift of cascaded amplifier of these 3-stages. [6+4+6]

6. (a) An N-channel JFET having V_P = - 4V and I_{DSS} = 12 ma is used as common source FET amplifier with potential divider biasing circuit. The parameter values are V_{DD}=24V. R_S = 1KΩ ; R_L = 1.25KΩ ; R_1 = 450KΩ and R_2 = 90KΩ . Draw the circuit with these parameters and explain the circuit working as amplifier
   (b) Draw the D.C equivalent circuit of the above amplifier circuit and determine the values of drain current I_D and V_{DS}. [8+8]

7. (a) Explain the effects on
      i. Noise
      ii. Nonlinear distortion and
      iii. Bandwidth of amplifiers with the introduction of voltage series feedback into the amplifiers
   (b) An amplifier with an open-loop voltage gain A_V of -1000 delivers 10 watts of output power at 10% second harmonic distortion, when the input signal is 10mv. If 40 db negative voltage-series feedback is applied and the output power is to remain at 10 watts; calculate
      i. the required input signal
      ii. percentage second harmonic distortion and
      iii. Closed-loop voltage gain.

   [8+8]

8. (a) Explain the phenomenon of piezoelectric effect associated with Quartz Crystals.
   (b) Draw the electrical equivalent circuit of a Quartz Crystal
   (c) Draw the graph showing the variation of crystal impedance as a function of frequency.
   (d) Discuss the stability of frequency of crystal oscillator circuits [4x4]

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Code No: RR221401 **Set No. 2**

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(Mechatronics)

Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
All Questions carry equal marks

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1. (a) Derive the expression for the barrier potential Vo at the junction of a P-N diode
   (b) Explain the situation for the occurrence of the phenomenon of Avalanche breakdown in semiconductor diodes and discuss the consequences.
   (c) Draw the equivalent circuit of a Semiconductor diode and briefly explain, how the diode acts as a switch. [6+5+5]

2. (a) With suitable sketches, discuss about the principle of operation of bridge rectifier circuit. Mention the advantages and disadvantages of the circuit when compared to other full wave rectifier circuit.
   (b) Derive the expressions for ripple factor and efficiency of bridge rectifier circuit. [8+8]

3. (a) Draw a diagram showing Various currents in a NPN Transistor in Common Base mode.
   (b) Draw a circuit to obtain the characteristics of a NPN Transistor in CB configuration
   (c) Draw the input and output characteristics of a Common Base Transistor.
   (d) Explain the operation of a NPN Bipolar Junction Transistor in CB configuration. [3+3+4+6]

4. (a) Draw the circuit diagrams showing the three configurations of Transistor amplifiers.
   (b) Draw the Transistor biasing circuit using Collector-to-base bias arrangement. Explain the concept of providing proper bias for the Transistor to act as amplifying device
   (c) Mention the DC load line equation for CE Transistor Collector to base bias circuit and describe the method of drawing the DC load line on the CE Transistor output characteristics. [6+6+4]

5. (a) Draw an R-C coupled amplifier circuit with two stages and explain its operation.
   (b) Draw the Frequency response of an R-C coupled amplifier. Show the method of determination of low frequency cut-off point f_1 or f_L and high frequency cut-off point f_2 or f_H and mark the various regions of operation on the frequency response.

(c) The maximum voltage gain A_{VM} of an Amplifier is 1000 over midband range. The voltage gain falls to 707 at 100 HZ and 22.1 KHZ . Determine the low frequency cut-off, high frequency cut-off and the amplifier bandwidth mentioning relevant concepts. [6+4+6]

6. (a) Draw the FET amplifier circuit with potential divider biasing with tabilization of bias. ssume sinusoidal input to the amplifier. Explain the operation of the amplifier showing the signal waveforms on the output characteristics of the device and the load line.

   (b) Discuss the concept of amplification from the small signal low frequency equivalent circuit of FET amplifier with necessary derivation for voltage amplification. [10+6]

7. (a) Mention the two types of feedbacks in electronic amplifiers. Explain the basic concepts of feedbacks using block diagrams and derive the expressions for overall gains

   (b) Draw the circuit diagram of a negative voltage feedback amplifier and explain its working with necessary details.

   (c) An amplifier with voltage gain of 60 decibels uses 0.05 of its output voltage in negative feedback. Calculate the gain of the feedback amplifier. [6+6+4]

8. (a) Draw the Wein Bridge oscillator circuit using a non-inverting amplifier. Derive the condition for the frequency of oscillations.

   (b) Determine the oscillation frequency of Wein Bridge oscillator with the lead-lag Circuit having $R_1 = R_2 =$ R =10 KΩ ; $C_1 = C_2 =$ C = 0.01μ f.

   (c) Calculate the frequency of oscillation f_0 of an RC phase shift oscillator using FET device using three-stage ladder network with R=1KΩ and C=1μ f. [10+3+3]

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Code No: RR221401 **Set No. 3**

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Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
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1. (a) Discuss the reasons for the formation of 'Transition Region' in P-N junction diode.
   (b) Discuss the impact of forward and reverse bias voltages applied to semiconductor diodes on the Transition region widths and junction capacitances.
   (c) State "Zener break down" and explain, how zener diode acts as a voltage regulator. [4+6+6]

2. (a) Discuss the functioning of rectifier circuits in DC sources for Electronic circuits.
   (b) Draw the circuit diagram of Full Wave rectifier using two semiconductor diodes and explain its working principle.
   (c) Mention the expression for rectification efficiency
   (d) Derive the expression for rectification efficiency [3+7+3+3]

3. (a) Draw the circuit diagram with biasing voltages to obtain UJT device characteristics.
   (b) Draw the UJT device characteristics and show the various regions with necessary explanation.
   (c) With suitable circuit diagram, explain how UJT can be used as relaxation oscillator. [4+6+6]

4. (a) Draw the circuit diagrams showing the three configurations of Transistor amplifiers.
   (b) Draw the Transistor biasing circuit using Collector-to-base bias arrangement. Explain the concept of providing proper bias for the Transistor to act as amplifying device
   (c) Mention the DC load line equation for CE Transistor Collector to base bias circuit and describe the method of drawing the DC load line on the CE Transistor output characteristics. [6+6+4]

5. (a) Draw the practical circuit of a single stage Common Emitter Transistor Amplifier with voltage divider biasing.
   (b) Assuming sinusoidal input signal to the above CE Transistor amplifier, explain the working of the amplifier with necessary waveforms.

(c) Draw the A.C load line on the output characteristics of the CE Transistor and explain the concept of amplification and 180^0 phase shift between input and output signals. [4+4+8]

6. (a) Draw the potential divider bias circuit for P-Channel JFET and explain the function of each component in the circuit.

   (b) Derive the expression for voltage gain of JFET model for self bias configuration. [8+8]

7. (a) Draw the four topologies of negative feedback amplifiers; clearly showing the types of sampling and mixing of signals for each type of feedback amplifiers.

   (b) Calculate the gain of a negative feedback amplifier having A = 450 and β = 0.02.

   (c) If an amplifier with gain of - 500 and feedback factor β = -0.2 has a gain change of 25% due to changes in temperatures. Calculate the change in gain of he feedback amplifier. [8+4+4]

8. (a) Draw the Wein Bridge oscillator circuit using a non-inverting amplifier. Derive the condition for the frequency of oscillations.

   (b) Determine the oscillation frequency of Wein Bridge oscillator with the lead-lag Circuit having $R_1 = R_2$ = R =10 KΩ ; $C_1 = C_2$ = C = 0.01μ f.

   (c) Calculate the frequency of oscillation f_0 of an RC phase shift oscillator using FET device using three-stage ladder network with R=1KΩ and C=1μ f. [10+3+3]

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1. (a) Discuss the significance of Forbidden Band Gap energy in Energy-Band Diagrams with reference to the difference in cut-in voltages for Silicon and Germanium diode working under forward Bias conditions.
   (b) Mention the reason for Silicon devices to work at higher temperatures when compared to Germanium devices with necessary Energy Band diagrams.
   (c) Calculate the magnitude of barrier voltage at 300^0K for P-N junction with N_A=10^{18}/cm^3 on P-side and N_D= 10^{15}/cm^3 on N-side of a Germanium semiconductor diode. Intrinsic carrier concentration n_i= 1.5x10^6/cm^3 and. V_T=25 mv at 300^0K. [6+6+4]

2. (a) Explain the application of a semiconductor diode as a rectifier.
   (b) Draw the input signal and output signal of a Half Wave rectifier circuit.
   (c) Derive the expression for V_{DC} and $V_{R.M.S}$ of H W R output signal.
   (d) Derive the expression for ripple factor 'γ ' of a Half Wave rectifier circuit. [3+3+4+6]

3. (a) Draw a diagram showing the input and output diode representation of a PNP Transistor with biasing voltages so that the Transistor can be operated as an amplifying device,
   (b) Discuss qualitatively the conditions of flow of currents through a PNP Transistor contributing to the fact that Emitter current is the sum of Collector and Base currents
   (c) Define 'α'. Derive the expression for alpha (α) in terms of Beta (β) of a Transistor
   (d) Draw a circuit for a Transistor to be operated as a Switch and explain its operation [4x4]

4. (a) Why biasing is necessary for a Transistor circuit in a given configuration. Mention the three different types of biasing a Bipolar Junction Transistor.
   (b) Draw the Transistor biasing circuit using fixed bias arrangement and explain its principle with suitable analysis.
   (c) Mention the DC load line equation for CE Transistor fixed bias circuit and describe the method of drawing the DC load line on the CE Transistor output characteristics. [6+6+4]

5. (a) Discuss the advantages and disadvantages of R-C coupled transistor amplifiers. What is the role of coupling capacitor in determing the frequency response.

   (b) Derive the expression for gain-bandwidth product of the amplifier and show that the gain-bandwidth product is constant. [8+8]

6. (a) An N-channel JFET having V_P = - 4V and I_{DSS} = 12 ma is used as common source FET amplifier with potential divider biasing circuit. The parameter values are V_{DD}=24V. R_S = 1KΩ ; R_L = 1.25KΩ ; R_1 = 450KΩ and R_2 = 90KΩ . Draw the circuit with these parameters and explain the circuit working as amplifier

   (b) Draw the D.C equivalent circuit of the above amplifier circuit and determine the values of drain current I_D and V_{DS}. [8+8]

7. (a) How does negative feedback stabilize the gain of the amplifiers?

   (b) Derive an expression showing the reduction of nonlinear distortion in amplifiers when negative feedback is introduced into it.

   (c) In an amplifier, the total distortion 'D' is 10% and the voltage gain A_V is 2250.
   Calculate the amount of negative feedback for the harmonic distortion in the feedback amplifier to be 1%. Calculate the voltage gain A_{Vf} of the feedback amplifier also. [4+4+8]

8. (a) Draw the Wein Bridge oscillator circuit using a non-inverting amplifier. Derive the condition for the frequency of oscillations.

   (b) Determine the oscillation frequency of Wein Bridge oscillator with the lead-lag Circuit having $R_1 = R_2$ = R =10 KΩ ; $C_1 = C_2$ = C = 0.01μ f.

   (c) Calculate the frequency of oscillation f_0 of an RC phase shift oscillator using FET device using three-stage ladder network with R=1KΩ and C=1μ f. [10+3+3]

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