Code No: NR220501 **NR**

II B.Tech II Semester Supplementary Examinations, November/December 2005
COMPUTER ORGANISATION
(Common to Computer Science & Engineering, Information Technology, Computer Science & Systems Engineering and Electronics & Computer Engineering)

Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
All Questions carry equal marks

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1. (a) Explain the architecture of Von Neumann machine clearly.
   (b) Prove that the multiplication of two n-digit numbers in base B gives a product of no more than 2n digits. [8+8]

2. (a) Explain Pentium Addressing Modes with an example
   (b) Let the address stored in the program counter is designated by the symbol X1. The instruction stored in X1 has an address part X2. The operand needed to execute the instruction is stored in the memory word with address X3. An index register contains the value X4. What is the relationship between these various quantities if the addressing mode of the instruction is
      i. direct
      ii. indirect
      iii. PC-relative and
      iv. Indexed [10+6]

3. (a) List and explain, how instructions are classified in 8085. Give example for each classification
   (b) Write a program for 8085 microprocessor to,
      i. Load 00H in the accumulator from a memory location
      ii. Decrement the accumulator
      iii. Store the result to next memory location [10+6]

4. Consider an accumulator based CPU with the following eight one address instructions. LOAD X, STORE X, ADD X, AND X, JMP X, JMPZ X, CMPL, (Complement Accumulator), and RSHIFT. Give fetch and execute cycle operations and identify the necessary control signals to be generated for the above instructions by a micro programmed control unit. [16]

5. (a) Describe how the information is recorded in Magnetic tape.
   (b) Explain how cache memories can be used in paging technique. [8+8]

6. (a) What do you mean by thrashing?

(b) Explain how number of page faults can be calculated for the given page trace using LRU page removal technique. (Assume 4 frames are available in the memory). [6+10]

7. (a) What is a Bus? Discuss two typical bus structures.

   (b) What are different types of I/O devices? Discuss the advantages of using I/O processor. [8+8]

8. (a) Differentiate between programmed I/O and memory mapped I/O.

   (b) Compare interrupt I/O control with DMA I/O control. Why does DMA have priority over CPU when both requests a memory transfer? [6+10]

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