Code No: NR221103 **NR**

**II B.Tech II Semester Supplementary Examinations,**
**November/December 2005**
**DIGITAL CIRCUITS DESIGN AND APPLICATION**
**(Bio-Medical Engineering)**

**Time: 3 hours** **Max Marks: 80**

**Answer any FIVE Questions**
**All Questions carry equal marks**

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1. (a) A symmetrical square wave whose average value is zero has a peak-to-peak amplitude of 20V and a period of 2 $\mu$sec. This waveform is applied to a low-pass circuit whose upper 3-dB frequency is $\frac{1}{2\pi}$ MHz. Calculate and sketch the steady state output waveform. [8]

   (b) The input Voltage $V_i$ to the two-level clipper shown in figure 1 varies linearly from 0 to 150V. Sketch the output voltage $V_0$ to the same time scale as the input voltage. Assume ideal diodes. [8]

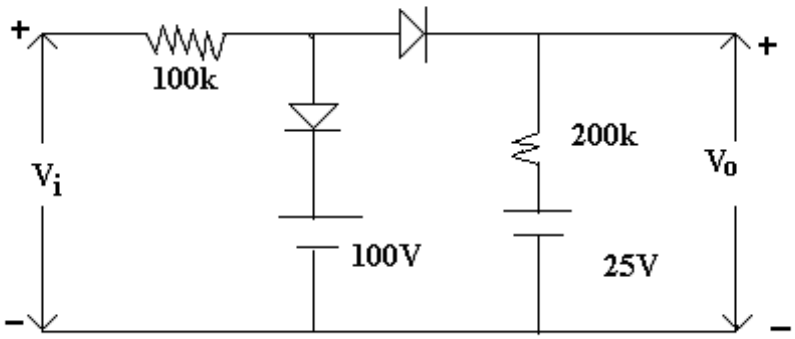


Figure 1:

2. Consider a collector-coupled astable multi using npn transistors. The circuit and device parameters are $V_{cc}$ = 15 V , $R_c$=3K, $R_1$=40K, $R_2$=20K, $h_{fe}$=30, $\gamma_{bb}$ = 0, $I_{CBO}$=0, and all forward-biased junction voltages may be neglected.
   calculate and plot the waveforms at the base and collector of one transistor. If the multi is oscillate at a frequency of 5 KHz, what is the value of the coupling capacitance? [16]

3. (a) Draw the functional schematic of a 555 timer and explain its operation . [10]

   (b) Explain any two applications of 555 timer in detail. [6]

4. (a) Encode the decimal numbers into

   i) $(56)_{10}$ = ( $)_{Graycode}$
   ii) $(20.305)_{10}$ = ( $)_{excess-3code}$
   iii) $(32.89)_{10}$ = ( $)_{BCD\ code}$ [6]

(b) Simplify the logic expression using K.map .
f=ABC+B$\overline{C}$D+$\overline{A}$ BC
and realize 'f' using NAND gates only. [10]

5. (a) Using tabulation procedure find set of prime implements and obtain a minimal expression for the following.
$f(w,x,y,z) = \Sigma(1,5,6,7,9,13,14,15,17,18,19,20,25,29,30)$ [10]

(b) Draw the block schematic of 4x1 MUX and give its truth table. [6]

6. (a) Design a full adder with minimum number of NAND gates. [8]

(b) Draw the logic diagram of 1 to 4 line demultiplexer and explain its operation. [8]

7. (a) Design a modulo-6 counter using NAND gates and JK flip flops. [8]

(b) Draw C-MOS inverter and explain its operation and give typical input and output voltages of $V_{DD} = 5V$ [8]

8. Write short notes on any three topics: [5+5+6=16]

(a) LED Displays

(b) Dot matrix display

(c) PLL ICs

(d) TTL gates

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