Code No: RR222201 **Set No. 1**

II B.Tech II Semester Supplementary Examinations, November/December 2005
SWITCHING THEORY AND LOGIC DESIGN
(Instrumentation & Control Engineering)

Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
All Questions carry equal marks

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1. (a) Devise a single error correcting code for a 11 bit group 01101110101
   (b) Test the following Hamming code sequence for 11 bit message and correct it if necessary (1010010111 01011).

   [8+8]

2. (a) Simplify the function using Karnaugh map method F (A,B,C,D) = $\sum$(4,5,7,12,14,15)+ $\sum$d(3,8,10).
   (b) Give three possible ways to express the function F = $\overline{A}\ \overline{B}\ \overline{D} + \overline{A}\ \overline{B}\ \overline{C}\ \overline{D} + \overline{A}BD + AB\overline{C}D$ with eight or less literals.

   [8+8]

3. (a) Minimize the given multiple output function whose truth table is given below

X	Y	Z	F	G
0	0	0	0	1
0	0	1	0	1
0	1	0	0	0
0	1	1	1	1
1	0	0	0	0
1	0	1	0	0
1	1	0	1	0
1	1	1	1	0

   x,y,z are inputs and F , G are outputs

   (b) Draw a logic diagram using only two-input NAND gates to implement the following expression.
   (AB+$\overline{A}\ \overline{B}$)(C$\overline{D} + \overline{C}$ D)

   [8+8]

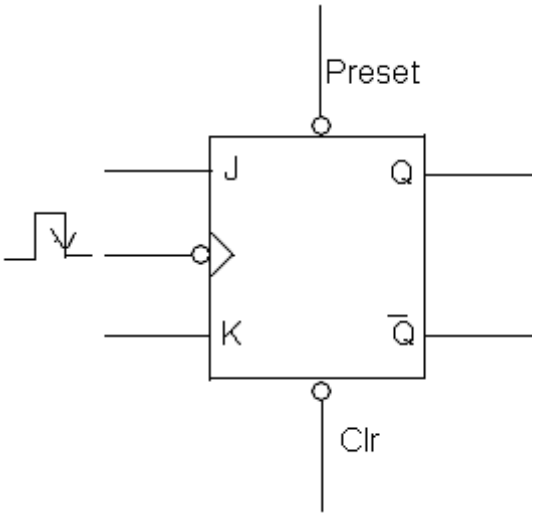
4. (a) Give the schematic circuit for a BCD-to-decimal decoder. Give the truth-table for the same.
   (b) A combinational circuit is specified by the following two Boolean functions Design the circuit with a decoder and basic gates.
   F = $\sum$ m (1,5,9,15)
   G = $\sum$ m (0,1,9,10,12)

   [8+8]

5. (a) Define the following terms with related to Flip-Flop

i. set-up time
ii. hold-time
iii. propagation delay-time

(b) for the block diagram shown, draw the schematic circuit usinf NAND gates and explain its operation with help of truth-table.



[6+10]

6. (a) Compare merits and demerits of ripple and synchronous counters.
   (b) Design a modulo-12 up synchronous counter using T-flip flops and draw the circuit diagram.

[6+10]

7. For the machine shown in the table below obtain:
   (a) The corresponding reduced machine table in standard form
   (b) Find a minimum length that distinguishes state A from state B where PS: present state, NS: next state, Z: output, X: input

PS	NS,Z	
	X=0	X=1
A	B,1	H,1
B	F,1	D,1
C	D,0	E,1
D	C,0	F,1
E	D,1	C,1
F	C,1	C,1
G	C,1	D,1
H	C,0	A,1

[10+6]

8. Obtain the ASM charts for the following state transition

   (a) If x = 0, control goes from T1 to state T2, if x = 1, generate the conditional operation and go from T1 to T2.

   (b) If x = 1, control goes from T1 to T2 and then to T3, if x = 0, control goes from T1 to T3.

   (c) Start from state T1, then if xy = 00, go to T2, if xy = 01, then go to T3, if xy = 10, then go to T1, otherwise go to T3. and design its control circuit using

      i. D flip flop & decoder

      ii. Input multiplexer & a register

[8+8]

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1. (a) Perform the subtraction with the following unsigned binary numbers by taking the 2's complement of the subtrahend.
   i. 11010-10000
   ii. 11010-1101
   iii. 100-110000
   iv. 1010100-1010100
   (b) The binary numbers listed have a sign bit in the left most position and, if negative, are in 1's complement form. Perform the arithmetic operations indicated and verify the answers.
   i. 101011+111000
   ii. 001110+110010
   iii. 111001-001010
   iv. 101011-100110

[8+8]

2. (a) Minimise the following expression using Karnaugh -map
   f (A,B,C,D) =$\sum$m (1,4,7,10, 13) +$\sum$d (5,14,15)
   (b) Find the complement and dual of the function below and then reduce it to a minimum number of literals in each case. f = [$(\overline{ab})$a][$(\overline{ab})$b].

[8+8]

3. (a) Derive Boolean expression for a 2 input Ex-NOR gate to realize with two input NOR gates, without using complemented variables and draw the circuit.
   (b) Redraw the given circuit (figure1) after simplification.

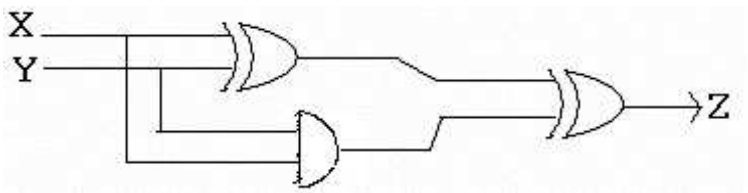


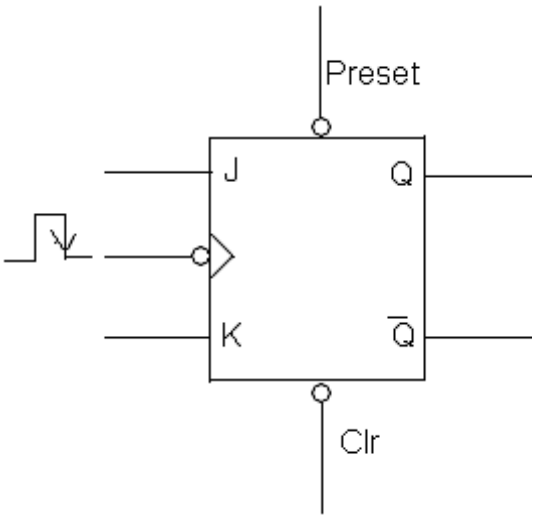
Figure 1:

[8+8]

4. (a) Give the implementation of a 4-bit ripple-carry adder using half- adder(s) / full-adder(s).
   (b) Explain with an example , the mux and demux can be used as data - selector and data-distributor respectively.

[8+8]

5. (a) Define the following terms with related to Flip-Flop
      i. set-up time
      ii. hold-time
      iii. propagation delay-time
   (b) for the block diagram shown, draw the schematic circuit usinf NAND gates and explain its operation with help of truth-table.



[6+10]

6. Design a counter which could count either in mod 8 straight binary or in mod 8 cyclic code based on a control signal. [16]

7. For the machine shown in the table below obtain:
   (a) The corresponding reduced machine table in standard form
   (b) Find a minimum length that distinguishes state A from state B where PS:

present state, NS: next state, Z: output, X: input

PS	NS,Z	
	X=0	X=1
A	B,1	H,1
B	F,1	D,1
C	D,0	E,1
D	C,0	F,1
E	D,1	C,1
F	C,1	C,1
G	C,1	D,1
H	C,0	A,1

[10+6]

8. (a) Design a digital system with three 4-bit registers, A, B and C to perform the following operations by drawing the ASM chart.
   i. Transfer two binary numbers to A and B when a start signal is enabled.
   ii. If A<B, shift left the contents of A and transfer the result to register C.
   iii. If A>B, shift right the contents of B and transfer the result to register C.
   iv. If A+B, transfer the number to register C unchanged.

   (b) Realize the above using JK flipflops and D flip flops.

[8+8]

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1. (a) Perform the subtraction with the following unsigned binary numbers by taking the 2's complement of the subtrahend.
   i. 11010-10000
   ii. 11010-1101
   iii. 100-110000
   iv. 1010100-1010100
   (b) The binary numbers listed have a sign bit in the left most position and, if negative, are in 1's complement form. Perform the arithmetic operations indicated and verify the answers.
   i. 101011+111000
   ii. 001110+110010
   iii. 111001-001010
   iv. 101011-100110

   [8+8]

2. (a) i. Obtain the simplified sum of products expression for the function $F(k,l,m,n) = \overline{k}lm + \overline{k}\ \overline{m}n + kl\overline{m}\ \overline{n} + lm\overline{n}$
   ii. Simplify $A + \overline{A}B + \overline{B}C + \overline{C}D$
   (b) Find the minimal sum of products expression for f(w,x,y,z) = $\sum$(0,2,4,9,12,15) +$\sum \phi$(1,5,7,10) using Karnaughs- map

   [8+8]

3. Using the Quine-Mc Cluskey method of tabular reduction ,minimize the given combinational single - output function f(w,x,y,z) = $\sum$m(0,1,5,7,810,14,15) [16]

4. (a) Give the schematic circuit for a BCD-to-decimal decoder. Give the truth-table for the same.
   (b) A combinational circuit is specified by the following two Boolean functions Design the circuit with a decoder and basic gates.
   F = $\sum$ m (1,5,9,15)
   G = $\sum$ m (0,1,9,10,12)

   [8+8]

5. (a) Analyze the circuit(figure1) given and prove it is equivalent to a T flip flop.

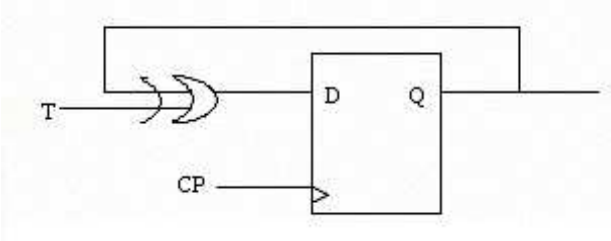

Figure 1:

(b) Draw the circuit diagram of a mod-10 ripple counter and explain its operation with the aid of output state timing diagram.

[6+10]

6. Design a synchronous decimal counter to count in excess-3 code. Use T flip flops. [16]

7. (a) Distinguish between Melay and Moore machines.

   (b) Find the equivalence partition for the given machine and a standard form of the corresponding reduced machine.

PS	NS,2	
	X=0	X=1
A	$B_1 0$	$E_1 0$
B	$E_1 0$	$D_1 0$
C	$D_1 1$	$A_1 0$
D	$C_1 1$	$E_1 0$
E	$B_1 0$	$D_1 0$

[4+12]

8. Construct an ASM block that has 3 input variables (A,B,C), 4 output (W,X,Y,Z) and 2 exit paths. For this block, output Z is always 1, and W is 1 if A & B are both 1. If C=1 & A=0, Y=1 and exit path 1 is taken. If C=0 or A=1, X=1 and exit path 2 is taken.
   Realize the above using the One flip flop per state. [16]

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1. (a) A person on SATURN possessing 18 fingers has a property worth (1,00,000)18. He has 3 daughters and two sons. He wants to distribute half the money equally to his sons and the remaining half to his daughters equally. How much his each son and each daughter will get in Indian currency?
   (b) An Indian started on an expedition to SATURN with Rs.1,00,000. The expenditure on SATURN will be in the ratio of 1:2:7 for food, clothing and traveling. How much he will be spending on each item in the currency of SATURN.

   [8+8]

2. (a) Find the minimal expression for the function f(w,x,y,z)=$\sum$(0,2,5,9,15) +$\sum$d (6,7,8,10,12,13) using Karnaughs-map.
   (b) i. Determine the Canonical sum-of-products form for $T(x, y, z) = \overline{x}y + \overline{z} + xyz$
   ii. Minimize the function $f(x, y, z, w) = x + xyz + wx + \overline{x}y + \overline{w}x + \overline{x}yz$.

   [8+4+4]

3. Using the tabular method, obtain the prime implicants of a four- input single-output function f(w,x,y,z) = $\sum$m(0,2,4,5,6,7,8,9,10,11,13). Reduce the prime-implicant table and find the minimal cover of f. [16]

4. (a) Show how a 16-to-1 mux can be realized using 4-to-1 muxes.
   (b) Implement the function f(a,b,c)= a.b + $\bar{b}$.c using the 4-to-1 mux.

   [8+8]

5. (a) What is the race around condition in flip-flops. Explain with the help of example.
   (b) Give transition tables for the given flop-flops J-K, R-S, T and D-Flip-Flops
   (c) Draw the circuit of positive edge trigger J-K flip-flop with active high preset and active low clear and explain its operation with the help of Truth-Table.

   [6+4+6]

6. (a) Draw the state diagram for the synchronous sequential circuit with inputs (x_1, x_2) and single output z in which the input pair represents alphabet letters as given below.
   A-00
   B-01

C-10
D-11

The output is 1 if the most recent two inputs are in alphabetic order (i.e.) AB, BC and CD.

(b) Draw the circuit diagram of R-S flip flop with active low preset and clear with level mode clock. What is the disadvantage in using level mode clock? How to overcome this problem. Discuss.

[8+8]

7. (a) Convert the following Mealy machine into a corresponding Moore machine:

PS	NS,Z	
	X=0	X=1
A	C,0	B,0
B	A,1	D,0
C	B,1	A,1
D	D,1	C,0

(b) Design the circuit for the above table.

[8+8]

8. (a) Explain how the ASM chart differs from a conventional flow chart. Using an example show the difference in interpretation.

(b) Obtain the ASM charts for the following state transition

i. If x = 0, control goes from T1 to state T2, if x = 1, generate the conditional operation and go from T1 to T2.

ii. If x = 1, control goes from T1 to T2 and then to T3, if x = 0, control goes from T1 to T3.

iii. Start from state T1, then if xy = 00, go to T2, if xy = 01, then go to T3, if xy = 10, then go to T1, otherwise go to T3.

[8+8]

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