

**II B.Tech. II Semester Supplementary Examinations,
November/December -2005
COMPUTER ORGANIZATION
(Common to Computer Science & Engineering, Information
Technology, Computer Science & Systems Engineering and Electronics &
Computer Engineering)**

Time: 3 hours

Max Marks: 80

**Answer any FIVE Questions
All Questions carry equal marks**

1. (a) Explain in detail about the PCI bus Arbitration.
(b) Draw and Explain about the Von Neumann architecture.
2. (a) Explain about the pentium and power PC operation types.
(b) What is the Branch prediction? What are the approaches of Branch Prediction? Draw and Explain about the Branch Prediction flow chart.
3. (a) Explain in detail about any four addressing modes with examples.
(b) Explain about the PDP-8 and PDP-10 Instruction formats.
4. (a) What is the cache memory principle? Explain about the cache read operation.
(b) What is the need of mapping function in cache design? Explain about the direct mapping, associative mapping and set associative mapping.
5. (a) Explain about the various partition techniques used in memory management.
(b) What is Demand Paging? What are the disadvantages of paging Techniques?
(c) What is meant by memory Inter leaving?
6. (a) Distinguish between the programmed I/O and memory mapped I/O.
(b) Explain in detail about programmable peripheral Interrupt controller.
7. (a) Explain three broad classification of external or peripheral, devices.
(b) List and briefly define three techniques for performing I/O.
(c) When a DMA module takes control of a bus, and while it retains control of the bus, what does the processor do?
8. (a) Explain about Vertical and Horizontal Instructions.
(b) Explain in detail about the Micro Instruction Encoding.

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1. (a) Explain in detail about the PCI Data transfers with the neat diagram.
(b) Explain about
 - i. Fixed point representation.
 - ii. Signed magnitude representation of numbers.
2. (a) Explain about the Pentium and Power PC Data Types.
(b) What is Instruction Pipelining? Explain Two stage and six stage CPU Instruction pipeline with diagrams.
3. (a) Explain in detail about the logical, transfer of control and Arithmetic Operations.
(b) Explain in detail about the Register Organization.
4. (a) Explain about
 - i. Sequential Access
 - ii. Direct Access
 - iii. Random Access
 - iv. Associative Access.
(b) Explain the Memory Hierarchy.
(c) What is the Principle of locality of Reference?
5. (a) Why are Associative memories needed?
(b) What are the uses of magnetic Tapes?
(c) What are the operations performed to manage memory?
6. (a) Explain about the programmed I/O. What are the I/O commands used in programmed I/O.
(b) What is cycle stealing? Draw and explain about the typical DMA Block diagram.
7. (a) Write about the evolution of the I/O functions.
(b) Write about the characteristics of I/O channels.

- (c) What is I/O processor?
8. Explain about:
- (a) Instruction Pipeline.
 - (b) Parallel Processing.
 - (c) Problems in Parallel Processing, and
 - (d) Intel 80486 Pipelining.

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1. (a) List and briefly explain the functional groups of signal lines for PCI.
(b) What is the benefit of using a multiple bus structure compared to a single bus architecture?
2. (a) Draw and explain about the Instruction cycle state diagram.
(b) What is Instruction format? Explain about the pentium and power PC Instruction Formats.
3. (a) Explain in detail about the Data Transfer, conversion and system control operations.
(b) Draw and explain the Internal structure of the CPU.
4. (a) Explain about the various types of Random Access Semiconductor Memories.
(b) Explain the Memory cell operation.
(c) Explain about
 - i. Access Time
 - ii. Memory Cycle Time.
5. (a) Draw and Explain about the Virtual Memory Organization.
(b) Explain about Virtual Memory Address Translation.
(c) Explain about the usage of TLB.
6. (a) Explain about the I/O Module Functions.
(b) In virtually all systems that include DMA modules, DMA access to Main Memory is given higher priority than CPU access to Main Memory. Why?
7. (a) Write in detail about the classification of External Devices.
(b) Write about DMA function.
(c) A DMA module is transferring characters to memory using cycle stealing from a device transmitting at 9600 bps. The CPU is fetching instructions at the rate of 1 MIPS. By how much will the processor be slowed down due to the DMA activity?

8. Describe three different micro instruction sequencing techniques with suitable examples.

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1. (a) Explain about Combinational and Sequential ALU's.
(b) Draw and explain a Timing diagram for PCI write Operation.
2. (a) Explain about the Pentium and Power PC Addressing modes.
(b) Explain about the Pentium Processor Register Organization. Write about EFLAGS Register.
3. (a) Explain about RISC characteristics.
(b) Write about RISC pipelining.
(c) What is a delayed branch?
4. (a) What is the need of replacement algorithm in cache design? Write about the LRU, FIFO, LFU and Random replacement Algorithms.
(b) What is write policy? Write about various write policies.
(c) What is Associative memory and what is its advantage?
5. (a) What is meant by segmentation? What are the advantages and disadvantages of segmentation.
(b) What is meant by compaction?
(c) Write about the Optical Disks.
6. (a) What is Interrupt Driven I/O? With the help of flow chart, explain about the sequence of events occur in Interrupt Processing.
(b) Write about the Design Issues arise in implementing Interrupt I/O.
7. (a) Give the typical Horizontal and Vertical Instruction formats.
(b) Describe how micro instructions are arranged on control memory and how they are interpreted.
8. Explain about:
(a) Data Hazard,
(b) Control Hazard,

- (c) PCI commands, and
- (d) Instruction Pipeline.

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