

III B.Tech. I Semester Regular Examinations, November -2005
MICROPROCESSORS AND INTERFACING
(Electronics & Computer Engineering)

Time: 3 hours

Max Marks: 80

Answer any FIVE Questions
All Questions carry equal marks

1. (a) Draw the block diagram of 8086 and explain each block?
(b) Discuss the addressing modes provided by 8086 and explain with examples?
[8+8]
2. (a) What are the different ways of passing parameters to and from procedures?
Explain the methods with examples in assembly language.
(b) Give the assembly language implementation of the following.
 - i. DO - WHILE
 - ii. FOR[10+6]
3. The I/O circuitry in an 8086 based system consists of five I/O devices with one status signal for each device. Design the required hardware providing two address locations to each device, one for status and other for data. In the range 0F00H to 0FOFH. Write an instruction sequence to test the status of each device and store it.
[16]
4. Write the necessary instruction sequence to initialize 8255 with address 0C00H to 0C03H for the following combinations.
 - (a) Port A as input port in mode 1 and port B as input port in mode 1 without the interrupt driven i/o.
 - (b) Port A in mode 2 as output port and port B as input port in mode 0 with interrupt driven i/o.
 - (c) Port A in mode 0, port c upper half as input ports and port B as input port in mode 1 with interrupt driven i/o.
 - (d) Port A as output port in mode 1 with active interrupt, port B as input port in mode 0 and port C lower half as output port in mode 0. [4 x 4 =16]
5. (a) Draw the command register and mode register format of 8237 and explain each bit?
(b) Show how 8237's are cascaded to provide more number of DRQ's and explain the operation?
(c) Explain how memory to memory transfer is performed with 8237? [5+6+5]
6. (a) Draw the block diagram of 8259 and explain each block?
(b) Explain how IRET instruction is executed? [12+4]

7. In an SDK-86 kit 128KB SRAM and 16KB EPROM is provided on system and provision for expansion of another 64KB SRAM is given. The on system SRAM address map is from 00000H to 1FFFFH and that of EPROM is from FC000H to FFFFFH. The expansion slot address map is from 80000H to 8FFFFH. The size of SRAM chip is 32KB. EPROM chip size is 8KB. Give the complete memory interface and also the address map for individual chips? [16]
8. Interface two 8255's to 8051 with starting address of 0F000H? Show the hardware design? Write the instruction sequence to initialize all ports of first 8255 as output ports in mode 0 and in the second 8255 port A as input in mode 1 and other ports as input in mode 0. [16]

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1. It is necessary to check whether the word stored in location 4000H:A000H is positive number or not? Show all possible ways of testing the above condition and store 00H if the condition is satisfied in location 3000:2002. Otherwise store 0FFH. [16]
2. (a) Develop an assembly language program to find the average of 'n' elements of an array of 4-digit hex numbers? Round off the average to digits position? The value of 'n' is available in location 'length'.
(b) Develop an assembly language program to convert 4-digit hex to BCD? [8+8]
3. Distinguish between a memory read and write machine cycle? Draw the timing diagrams in minimum and maximum modes of operation? [8+8]
4. Write the necessary instruction sequence to initialize 8255 with address 0C00H to 0C03H for the following combinations.
 - (a) Port A as input port in mode 1 and port B as input port in mode 1 without the interrupt driven i/o.
 - (b) Port A in mode 2 as output port and port B as input port in mode 0 with interrupt driven i/o.
 - (c) Port A in mode 0, port C upper half as input ports and port B as input port in mode 1 with interrupt driven i/o.
 - (d) Port A as output port in mode 1 with active interrupt, port B as input port in mode 0 and port C lower half as output port in mode 0. [4 x 4 =16]
5. (a) Distinguish between synchronous and asynchronous serial data transmission techniques? Discuss the advantages and disadvantages? [8]
(b) Draw the block diagram of combination of FAX and Data Modem? Explain each block? [4+4]
6. (a) Write an instruction sequence that will cause the priority of an 8259, whose even address is 0800H, to be IR_5 , IR_6 , IR_7 , IR_0 , IR_1 , IR_2 , IR_3 , IR_4 . Solve this problem when the current priority is IR_1 and for the second time assuming the current priority to be IR_7 ?
(b) Explain with examples how interrupt type 1 and type 3 provide debugging feature? [10+6]

7. In an SDK-86 kit 64KB SRAM and 32KB EPROM is provided on system and provision for expansion of another 64KB SRAM is given. The on system SRAM address map is from 00000H to 0FFFFH and that of EPROM is from F8000H to FFFFFH. The expansion slot address map is from 80000H to 8FFFFH. The size of SRAM chip is 32KB. EPROM chip size is 16KB. Give the complete memory interface and also the address map for individual chips? [16]
8. (a) Discuss the advantages of microcontroller based systems over microprocessor based systems?
- (b) Explain how 8051 is built around I/O ports? Discuss the function of each port in detail? [4+12]

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1. The register contents of 8086 is given below.

CS=5000H, DS=8000H, SS=9000H, ES=7000H, SI=1000H, DI=2000H, BP=0008H,
SP=0002H, AX=0000H, BX=5200H, CX=8000H, DX=2800H

Calculate the effective address and physical address of the following instructions.

- (a) MOV AX, [BP+BX-24D]
- (b) ADD AX, ES:[SI]
- (c) PUSH CX
- (d) SUB AX, [DI]
- (e) MOVSB
- (f) CMP AX, [DI]
- (g) ADD DX, [DI+8D]
- (h) MUL AX, [SI+2D] [16]

2. (a) Explain in detail the coding template for 8086 MOV instruction?
- (b) It is necessary to declare a program as a public procedure to be accessible by other programs? Give the sequence of assembly language statements? An external program called "fact" is to be used in this program. Show the required statements? [8+8]

3. What is the function of the ready pin in 8086. Draw the circuit diagram for wait state generation between 0 and 7 wait states and draw the corresponding timing diagram.

[16]

4. Explain why 8255 ports are divided into two groups? Discuss how these groups are controlled in different modes of operation? Explain different control signals and their associated pins for bi-directional I/O mode of operation? [4+6+6]

5. (a) Draw the flowchart showing how synchronous serial data can be sent from a port line using software routine?

- (b) Draw the block diagram of 8237 and explain each block. [8+8]

6. Explain the following terms with reference to 8259.

- (a) END of interrupt

- (b) Automatic rotation
 - (c) Poll command
 - (d) Read resister command. [4x4=16]
7. In an SDK-86 kit 128KB SRAM and 16KB EPROM is provided on system and provision for expansion of another 64KB SRAM is given. The on system SRAM address map is from 00000H to 1FFFFH and that of EPROM is from FC000H to FFFFFH. The expansion slot address map is from 80000H to 8FFFFH. The size of SRAM chip is 32KB. EPROM chip size is 8KB. Give the complete memory interface and also the address map for individual chips? [16]
8. An 8051 based system requires external memory of four 8Kbytes of SRAM each and two chips of EPROM of size 4Kbytes. The EPROM starts at address 1000H. SRAM address map follows EPROM map. Give the complete memory interface?

[16]

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2. (a) Give the assembly language implementation of the following.
 - i. DO WHILE
 - ii. FOR [4+4](b) What is a recursive procedure? Write a recursive procedure to calculate the factorial of number N, where N is a two-digit Hex number? [8]
3. (a) Compare interrupted I/O and DMA data transfer schemes.
(b) Describe the function of S_0 to S_7 pins of 8086 in maximum mode. [6+10]
4. Write the necessary instruction sequence to initialize 8255 with address 0C00H to 0C03H for the following combinations.
 - (a) Port A as input port in mode 1 and port B as input port in mode 1 without the interrupt driven i/o.
 - (b) Port A in mode 2 as output port and port B as input port in mode 0 with interrupt driven i/o.
 - (c) Port A in mode 0, port C upper half as input ports and port B as input port in mode 1 with interrupt driven i/o.
 - (d) Port A as output port in mode 1 with active interrupt, port B as input port in mode 0 and port C lower half as output port in mode 0. [4 x 4 =16]
5. (a) Discuss Overrun error and Framing error with reference to 8251?
(b) Discuss the mode instruction format of 8251 for synchronous and asynchronous mode of operation?
(c) Explain single transfer mode and block transfer mode of 8237? [5+5+6]
6. (a) Write an instruction sequence that will cause the priority of an 8259, whose even address is 0800H, to be $IR_5, IR_6, IR_7, IR_0, IR_1, IR_2, IR_3, IR_4$. Solve this problem when the current priority is IR_1 and for the second time assuming the current priority to be IR_7 ?
(b) Explain with examples how interrupt type 1 and type 3 provide debugging feature? [10+6]

7. (a) Discuss the organization of FLASH memory? Explain the FLASH memory command definitions?
(b) With the help of basic cell explain SRAM and DRAM? Discuss the advantages and disadvantages of the above memories? [6+10]
8. (a) Draw and discuss the formats and bit definitions of the following SFRs in 8051 microcontroller?
i. SCON
ii. TCON [4x2=8]
- (b) Discuss the following signal descriptions?
i. ALE/PROG
ii. \overline{EA}/V_{pp}
iii. \overline{PSEN}
iv. RXD [2x4=8]
