Code No: RR310401 **Set No. 1**

**III B.Tech I Semester Regular Examinations, November 2005**
**DIGITAL IC APPLICATIONS**
**(Electronics & Communication Engineering)**

**Time: 3 hours** **Max Marks: 80**

**Answer any FIVE Questions**
**All Questions carry equal marks**

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1. (a) Design a three input NAND gate using diode logic and a transistor inverter? Analyze the circuit with the help of transfer characteristics?
   (b) Compare HC, HCT, VHC and VHCT CMOS logic families with the help of output specifications with $V_{CC}$ from 4.5V to 5.5V? [10+6]

2. (a) Mention the DC noise margin levels of ECL 10K family?
   (b) A single pull-up resistor to +5V is used to provide a constant-1 logic source to 15 different 74LS00 inputs. What is the maximum value of this resistor? How much high state DC noise margin can be provided in this case? [8+8]

3. Explain with example the syntax and the function of the following VHDL statements
   (a) Process statement
   (b) If, else and elseif statements
   (c) Case statement
   (d) Loop statement [4x4=16]

4. With the help of logic diagram explain 74×157 multiplexer? Write the data flow style VHDL program for this IC? [8+8=16]

5. Design a 16-bit ALU using 74×381 and 74×182 ICs? [8+8]

6. (a) Draw the logic diagram of 74×74 IC and explain the operation? Develop the VHDL model for this IC?
   (b) With the help of logic diagram discuss PAL16R8? [8+8]

7. (a) Design a 3-bit LFSR counter using 74x194? List out the sequence assuming that the initial state is 001?
   (b) Explain with timing waveforms, different operations during one clock cycle in a synchronous system structure? [8+8]

8. (a) How many ROM bits are required to build a 16-bit adder/subtractor with mode control, carry input, carry output and twos complement overflow output. Show the block schematic with all inputs and outputs?
   (b) Design an 8x4 diode ROM using 74x138 for the following data starting from the first location?
   B,2,4,F,A,D,F,E [8+8]

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Code No: RR310401 **Set No. 2**

**III B.Tech I Semester Regular Examinations, November 2005**
**DIGITAL IC APPLICATIONS**
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**Time: 3 hours** **Max Marks: 80**

**Answer any FIVE Questions**
**All Questions carry equal marks**

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1. (a) Explain how to estimate sinking current for low output and sourcing current for high output of CMOS gate?
   (b) Analyze the fall time of CMOS inverter output with $R_L$ = 1K?, $V_L$ = 2.5V and $C_L$ = 100PF. Assume VL as stable state voltage. [8+8]
2. (a) Draw the circuit diagram of two-input 10K ECL OR gate and explain the circuit?
   (b) List out different categories of characteristics in a TTL data sheet? Discuss electrical and switching characteristics of 74LS00. [8+8]
3. Design a logic circuit to detect prime number of a 5-bit input? Write the structural VHDL program for the above design? [8+8=16]
4. (a) Using two 74×138 decoders design a 4 to 16 decoder?
   (b) Write a data flow style VHDL program for the above design? [8+8]
5. (a) Design a full subtractor with logic gates and write VHDL data flow program for the implementation of the above subtractor?
   (b) Using the above subtractor design a 8-bit ripple subtractor and write the corresponding VHDL program? [8+8]
6. (a) Design a switch debouncer circuit using 74×109 IC? Explain the operation using timing diagram?
   (b) Discuss the logic circuit of 74×377 register? Write a VHDL program for the above logic? [8+8]
7. (a) Design a 3-bit LFSR counter using 74×194? List out the sequence assuming that the initial state is 111?
   (b) Discuss in detail the synchronous system structure with a neat sketch? [8+8]
8. (a) Explain the internal structure of 64Kx1 DRAM? With the help of timing waveforms discuss DRAM access?
   (b) With a neat sketch, explain the general architecture of FPGA chip? What is the importance of configurable logic block? [8+8]

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Code No: RR310401 **Set No. 3**

**III B.Tech I Semester Regular Examinations, November 2005**
**DIGITAL IC APPLICATIONS**
**(Electronics & Communication Engineering)**

**Time: 3 hours** **Max Marks: 80**

**Answer any FIVE Questions**
**All Questions carry equal marks**

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1. (a) Draw the transistor logic inverter circuit and analyze the circuit behavior with the help of transfer characteristics?
   (b) Design a CMOS transistor circuit that has the functional behavior
   f (Z) = $\overline{(A+\bar{B})(B+C)}$ [8+8]

2. (a) Explain the difference in program structure of VHDL and any other procedural language? Give an example?
   (b) Explain sinking current and sourcing current of TTL output? Which of the above parameters decide the fanout and how? [8+8]

3. (a) Write a data-flow style VHDL program for the following functions?
   F(S) = A⊕B⊕$C_I$
   F($C_O$) = $AB$ + A⊕$C_I$ +$BC_I$ [4+4]
   (b) Explain with example the syntax and the function of the following VHDL statements?
      i. If, else and elseif statements
      ii. Case statement [8]

4. (a) Give the logic diagram of 74×139? Explain with the help of truth table? Using this device design a 3 to 8 decoder and provide the truth table?
   (b) Design a 16-bit comparator using 74×85 Ics? [8+8]

5. Draw the logic diagram of 74×283 IC and explain the operation? Write data flow VHDL program for this IC? [4+4+8]

6. With the help of logic diagram explain the function of PAL16R6? Explain how an 8-bit synchronous binary counter can be realized with this device? [8+8=16]

7. (a) Design an 8-bit parallel-in and serial-out shift register? Explain the operation of the above shift register with the help of timing waveforms?
   (b) Draw the logic diagram of 74×194 and explain the operation? [8+8]

8. (a) Explain the internal structure of 64Kx1 DRAM? With the help of timing waveforms discuss DRAM access?
   (b) Explain XC4000 programmable interconnect structure? [8+8]

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Code No: RR310401 **Set No. 4**

**III B.Tech I Semester Regular Examinations, November 2005**
**DIGITAL IC APPLICATIONS**
**(Electronics & Communication Engineering)**

**Time: 3 hours** **Max Marks: 80**

**Answer any FIVE Questions**
**All Questions carry equal marks**

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1. (a) Design a CMOS transistor circuit that has the functional behaviour f (Z) = $\overline{A.(B+C)}$
   (b) Design a 4-input CMOS AND-OR-INVERT gate? Draw the logic diagram and function table? [8+8]

2. (a) Draw the circuit diagram of basic TTL NAND gate and explain the three parts with the help of functional operation?
   (b) List out TTL families and compare them with reference to propagation delay, power consumption, speed-power product and low level input current? [8+8]

3. (a) Explain with example the syntax and the function of the following VHDL statements?
      i. If, else and elseif statements
      ii. Loop statement [4+4]
   (b) Design the logic circuit and write a data-flow style VHDL program for the following function?
      F (R) = $\Pi_{A,B,C,D}$ (1,4,5,7,9,13,15) [8]

4. Design a 10 to 4 encoder with inputs 1- out of 10 code and outputs in BCD? Provide the data flow style VHDL program? [8+8=16]

5. A 16-bit barrel shifter is a combinational logic circuit with 16-data inputs, 16-data outputs and 4-control inputs. The input word is rotated by a number of bit positions specified by control bits. Write a VHDL program for the above implementation? [16]

6. (a) Distinguish between latch and flip-flop? Show the logic diagram for both? Explain the operation with the help of function table? [4+4]
   (b) Design a conversion circuit to convert a T flip-flop to J-K flip-flop? [8]

7. (a) Explain LFSR? Design a4-bit LFSR using flip-flops and associated logic? List out all states with initial state as 0101?
   (b) Design an 8-bit serial-in and serial-out shift register? Write the data-flow style VHDL program for this shift register? [8+8]

8. (a) Explain the internal structure of 64Kx1 DRAM? With the help of timing waveforms discuss DRAM access?

(b) Explain XC4000 programmable interconnect structure? [8+8]

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