Code No: RR321202 **Set No. 1**

III B.Tech II Semester Supplementary Examinations,
November/December 2005
VLSI SYSTEMS DESIGN
(Information Technology)

Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
All Questions carry equal marks

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1. Implement the following gates with p-MOS transistors only and explain its working
   (a) 3 Input NAND gate.
   (b) Inverter. [8+8]
2. An p-MOS transistor is operating in the triode region with the following parameters $\mu_n Cox = 95\ \mu\ A/V^2$ W/L (ratio) = 90 $V_{gs} = -4V$, $V_{tn} = -1.1V$, $V_{ds} = -2V$. Find its drain current & drain -Source resistance. [16]
3. Explain with neat sketches CMOS fabrication using P - well process. [16]
4. Design a layout for CMOS 2-input NOR gate. [16]
5. Explain with suitable example how to design the layout of a gate to maximize performance and minimize area. [16]
6. Draw the structure of an un-signed array Multiplier and explain its working. [16]
7. Clearly explain about block placement and channel definition with respect to floor planning of the chip. [16]
8. Write a register-transfer description of one four-digit timer. [16]

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Code No: RR321202 **Set No. 2**

III B.Tech II Semester Supplementary Examinations,
November/December 2005
VLSI SYSTEMS DESIGN
(Information Technology)

Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
All Questions carry equal marks

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1. Implement the following logic functions using CMOS logic
   (a) $Y = \{(A+B)(C+D)\}^1$
   (b) $Y = \{AB+C\}^1$ [8+8]
2. Define different current parameters of Digital IC and explain their significance.[16]
3. Explain with neat sketches CMOS fabrication using twin - tub process. [16]
4. Design a layout for CMOS 2-input NAND gate. [16]
5. Explain clearly any one of the testing procedure to Test sequential Systems. [16]
6. Draw the circuit diagram of four transistor DRAM cell with storage nodes and explain its working. [16]
7. Clearly explain about block placement and channel definition with respect to floor planning of the chip. [16]
8. Explain about design methodology for 1BM ASICS. [16]

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Code No: RR321202 **Set No. 3**

III B.Tech II Semester Supplementary Examinations,
November/December 2005
VLSI SYSTEMS DESIGN
(Information Technology)

Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
All Questions carry equal marks

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1. Implement the following gates with p-MOS transistors only and explain its working
   (a) 2 Input AND gate.
   (b) 4 Input NOR gate. [8+8]
2. Name different IC fabrication technologies with suitable examples. [16]
3. Design a stick diagram for two-input N-MOS NAND and NOR gates. [16]
4. Explain about domino-logic and draw the transistor schematic of a two-input AND gate in domino logic. [16]
5. Explain the details of standard cell layout design method. [16]
6. Draw the circuit diagram of resistive load SRAM cell and explain its working principle. [16]
7. Explain clearly the global routing phase of the floor planning of the chip with few examples by considering all constraints. [16]
8. Design a block diagram for a PDP-8 data path that supports both one-bit and two-bit rotations. [16]

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Code No: RR321202 **Set No. 4**

III B.Tech II Semester Supplementary Examinations,
November/December 2005
VLSI SYSTEMS DESIGN
(Information Technology)

Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
All Questions carry equal marks

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1. Implement the following gates with CMOS Logic and explain its working
   (a) Ex-OR gate.
   (b) 2 Input NOR gate. [8+8]
2. (a) Define the terms SSI, MSI, LSI and VLSI.
   (b) Define the terms fan-out, fan-in, Propagation delay and noise margin of a logic-family. [8+8]
3. What is a stick diagram and explain about different symbols used for components in stick diagram. [16]
4. Design a layout for CMOS 3 - input OR gate. [16]
5. Explain in detail the path - delay measurement of the combinational logic circuits. [16]
6. Draw the structure of carry select adder and explain its working principle. [16]
7. Explain clearly block placement phase of the Floor planning of the chip with suitable examples. [16]
8. Draw the state transition graph for the kitchen timer chip's controller. [16]

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