Code No: NR321502 **NR**

III B.Tech II Semester Supplementary Examinations,
November/December 2005
ADVANCED COMPUTER ARCHITECTURE
(Computer Science & Systems Engineering)

Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
All Questions carry equal marks

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1. (a) Explain the requirement of large scale computations in substantiate the use of Numerical weather forecasting and large scale computation in Socio economics and Government use.
   (b) Explain the significance and necessity of Super computers in Engineering Design and Automation. [8+8]
2. Describe the Principles of Designing Pipeline Processors [16]
3. (a) Discuss the issues involved for Inter− PE Communication in array processors
   (b) What is a Multistage Network? Describe different types of multistage network. [8+8]
4. (a) Describe Batcher's Odd Even merge of two sorted sequences on a linear array of $PE's$ using an example.
   (b) Give the schematic logic design of a typical memory cell in an associative memory [8+8]
5. (a) Explain how two K-maps are connected in a cross-cluster memory access of a loosely coupled Multiprocessor.
   (b) Differentiate between Homogeneous Multiprocessors and Heterogeneous Multiprocessors [8+8]
6. (a) Explain briefly the different methods proposed to solve the cache coherence problem.
   (b) Explain briefly how multiprocessor operating systems are classified ? [10+6]
7. (a) Explain the organization of a static data flow computer.
   (b) What are the major design issues of a data flow computer? Explain in detail. [8+8]
8. (a) Give architecture of the front-end system interface with Cray-1 memory and functions sections.
   (b) Briefly explain the architecture of Cyber-205. [8+8]

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