Code No: RR322203 **Set No. 1**

III B.Tech II Semester Supplementary Examinations,
November/December 2005
MICROPROCESSORS & MICROCONTROLLERS
(Instrumentation & Control Engineering)

Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
All Questions carry equal marks

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1. (a) Give the 8085 compatible flags of 8086 processors? Discuss the design of each flag?
   (b) List out segmentation resisters of 8086? Explain how 8086 provides 1 MB memory address space using the segment registers? What is the purpose of extra segment? [8+8]

2. (a) Explain with example how a far procedure is declared as PUBLIC? Show how an external near procedure is called in main program?
   (b) Discuss the assembler directives with examples? [6+10]

3. What is function of ready pin in 8086. Draw the circuit diagram for wait state generation between 0 and 7 wait states and draw the corresponding timing diagram. [16]

4. It is necessary to initialize interrupt for mode 1 operation of port-A as input and port-B as output in the same mode with the 8255 address map of 0400H to 0700H. Give the complete hard ware design to interface 8255 to 8086 processor with this address map? Write the instruction sequence for the initialization of 8255 in the above modes? Give the instruction sequence to change the operation modes of port A, port C lower-half and Port B to mode 0 input ports? [16]

5. (a) Draw the circuit of TTL to RS232 and explain the necessity of this interface.
   (b) Draw necessary circuit to interface 8251 to an 8086 based system with an address 0A0H. Write the sequence of instructions to initialize 8251 for synchronous transmission with odd parity, single SYNC character, 8-bit data character? [6+10]

6. (a) What is the purpose of operational command words of 8259? Explain their format and the use?
   (b) What is type 2 interrupt? Explain the condition for initiating type 2 interrupt? What is the priority of this interrupt in 8086? [10+6]

7. It is necessary to interface 256KB SRAM and 64KB EPROM to an 8086 based system. The size of SRAM and EPROM chips is 32KB. Address map of SRAM is fixed from 00000H to 3FFFFH and that of EPROM is from F0000H to FFFFFH. Design the entire memory interface? Give the address map of individual chip?[16]

8. An 8051 based system requires external memory of four 8Kbytes of SRAM each and two chips of EPROM of size 4Kbytes. The EPROM starts at address 1000H. SRAM address map follows EPROM map. Give the complete memory interface?

[16]

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Code No: RR322203 **Set No. 2**

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Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
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1. (a) What is the use of trap flag? Discuss how trap flag provides debugging feature?
   (b) What is the difference between physical address, effective address and offset address? Explain with example how physical address is generated? [7+9]

2. (a) Explain in detail the coding template for 8086 MOV instruction? [8]
   (b) Write briefly about
      i. PUBLIC directive
      ii. EXTERN directive [4+4]

3. (a) Compare interrupted I/O and DMA data transfer schemes.
   (b) Describe the function of S_0 to S_7 pins of 8086 in maximum mode. [6+10]

4. Interface a 12-bit DAC to 8255 with an address map of 0C00H to 0C03H. The DAC provides output in the range of +5V to -5V. Write the instruction sequence.
   (a) For generating a square wave with a peak to peak voltage of 4V and the frequency will be selected from memory location 'F'.
   (b) For generating a triangular wave with a maximum voltage of +3V and a minimum of -2V. [6+10]

5. (a) Explain demand transfer mode and block transfer mode of 8237?
   (b) Show how 8237's are cascaded to provide more number of DRQ's and explain the operation?
   (c) Explain how memory to memory transfer is performed with 8237? [5+6+5]

6. (a) What are the five types of interrupts supported by 8086?
   (b) Write about interrupt vectors? How many bytes of memory does an interrupt vector requires?
   (c) Address 000E0H in the interrupt vector table contains 4132H and address 000E2H contains 0040H.
      i. To what interrupt type do these locations correspond?
      ii. What is the starting address for the interrupt service routine?[9+3+2+2]

7. (a) Design the required logic to generate read, write control signals for memory and I/O in a target system using 8086 microprocessor? Generate bank select signals for even and odd address memory banks?

(b) With the help of basic cell explain SRAM and DRAM? Discuss the advantages and disadvantages of the above memories? [8+8]

8. (a) Explain the internal RAM organization of 8051? Discuss how switching between register banks is possible? Give a sequence of instructions to switch from bank-0 to bank-2?

(b) What is the use of SFR? List out the special function registers of 8051? [10+6]

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Code No: RR322203 **Set No. 3**

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Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
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1. It is necessary to check the parity of the data byte in location 4000H:01FEH. If the parity is even store 00H otherwise store 0FFH in location 5000H:1000H. Give the instruction sequence for every addressing mode to achieve the above result. [16]

2. (a) Give the assembly language implementation of the following.
   i. DO WHILE
   ii. FOR [4+4]
   (b) What is a recursive procedure? Write a recursive procedure to calculate the factorial of number N, where N is a two-digit Hex number? [8]

3. The I/O circuitry in an 8086 based system consists of five I/O devices with one status signal for each device. Design the required hardware providing two address locations to each device, one for status and other for data. In the range 0F00H to 0FOFH. Write an instruction sequence to test the status of each device and store it. [16]

4. (a) What is BSR mode operation? How it is useful in controlling the interrupt initiated data transfer for mode 1 and 2?
   (b) Explain the transistor buffer circuit used to drive 7-segment LEDs? [8+8]

5. Write a program to initialize 8251 in synchronous mode with even parity, single SYNC character, 7 bit data character. Then receive 0FFH bytes of data from remote terminal and store it in the memory at address 2000H:2000H? [16]

6. (a) Write an instruction sequence that will cause the priority of an 8259, whose even address is 0800H, to be IR_5, IR_6, IR_7, IR_0, IR_1, IR_2, IR_3, IR_4. Solve this problem when the current priority is IR_1 and for the second time assuming the current priority to be IR_7?
   (b) Explain with examples how interrupt type 1 and type 3 provide debugging feature? [10+6]

7. (a) With a neat sketch explain the internal organization of SRAM chip? List out the input and output pins? Discuss their function in a system? [8]
   (b) Explain the following terms with reference to DRAM
   i. Write cycle
   ii. Access time

iii. Refresh

iv. Read cycle [4x2=8]

8. (a) How does 8051 differentiate between the external and internal program memory?

   (b) Explain how serial data communication is done with 8051 ports? [6+10]

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Code No: RR322203 **Set No. 4**

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Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
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1. (a) Explain why 8086 internal architecture is divided into BIU and EU? Discuss the A-bus, B-bus and C-bus and their use?
   (b) Explain the difference between memory segmentation and memory page? Why segmentation is useful in real-time applications? [8+8]

2. (a) Discuss various branch instruction of 8086 microprocessor, that are useful for relocation?
   (b) Using a do-while construct, develop a sequence of 8086 instructions that reads a character string from the keyboard and after pressing the enter key the character string is to be displayed again. [6+10]

3. (a) Explain how an 8086 enters into Wait State? How many wait states can be inserted in a machine cycle?
   (b) What is the difference between system bus cycle and bus idle cycle? Draw the timing diagram of bus idle cycle? [6+10]

4. It is necessary to initialize interrupt for mode 1 operation of port-A as input and port-B as output in the same mode with the 8255 address map of 0400H to 0700H. Give the complete hard ware design to interface 8255 to 8086 processor with this address map? Write the instruction sequence for the initialization of 8255 in the above modes? Give the instruction sequence to change the operation modes of port A, port C lower-half and Port B to mode 0 input ports? [16]

5. (a) How do we connect RS-232C equipment
      i. To data terminal type devices?
      ii. To serial port of SDK -86, RS-232C connection?
   (b) Give the specifications of RS-232C. [5+5+6]

6. Write an initialization sequence for an 8259 that is the only 8259 in an 8086 based system, with an even address of 0F0H that will cause.
   (a) Request to the edge triggered mode
   (b) IR_0 request to an interrupt type 30
   (c) SP/EN to output a disable signal to the data-bus transceivers.
   (d) The ISR bits to be cleared automatically at the end of second INTA pulse.

(e) The IMR to be cleared.

(f) The highest priority interrupt will be IR_6. [16]

7. (a) With a neat sketch explain the internal organization of SRAM chip? List out the input and output pins? Discuss their function in a system? [8]

   (b) Explain the following terms with reference to DRAM

   i. Write cycle
   ii. Access time
   iii. Refresh
   iv. Read cycle [4x2=8]

8. (a) Explain the internal RAM organization of 8051? Discuss how switching between register banks is possible? Give a sequence of instructions to switch from bank-0 to bank-2?

   (b) What is the use of SFR? List out the special function registers of 8051? [10+6]

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