Code No: RR321503 **Set No. 1**

III B.Tech II Semester Supplementary Examinations,
November/December 2005
FAULT TOLERANT SYSTEMS
(Computer Science & Systems Engineering)

Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
All Questions carry equal marks

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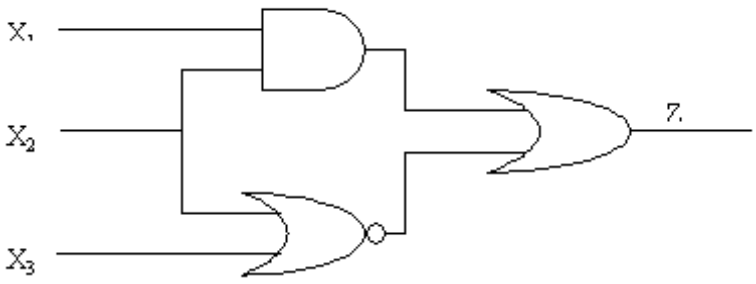
1. (a) If a system has 4000 identical components with a failure rate of 0.02% per 1000 hours. Find the MTBF of such a system.
   (b) Explain the phenomenon of Bath tub response for a Time Vs failure rate of a system. [8+8]

2. (a) Illustrate the principles of path sensitizing method for the circuit given below and generate test vectors for different paths having different faults on them as shown in the figure1.



$$Z = X_1X_2 + \overline{X}_2\overline{X}_3$$

Figure 1:

   (b) How is path sensitization method advantageous over Fault Table method.Prove it for the above example. [8+8]

3. (a) Explain fail soft-operation. [4]
   (b) Explain the 5 MR reconfiguration mechanism and also explain how it care tolerate single, double and Trible faults in a given system. [3x4=12]

4. (a) With an example explain the practical fault tolerant system?
   (b) How do you enhance the fault tolerance characteristics of digital systems.[8+8]

5. Design a totally self-checking checker for maximal-length Berger codes also give the procedure to generate test vectors of 8 bit long. [8+8]

6. Apply the procedure of designing a fail safe sequential machine using Berger code to the given state table. [16]

PS	NS, Z x=0	x=1
A	E,0	B,0
B	C,0	D,0
C	A,0	D,0
D	E,0	D,1
E	A,0	D,1

7. (a) What is meant by design for testability? What are the properties of a Design for testable circuit? Explain. [3+4+3]

   (b) How does controllability and observability take important role in design for testability? [3+3]

8. (a) Discuss the test patterns generated by Liner Feedback Shift Register.

   (b) What is meant by convolved LFSR/SR [8+8]

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Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
All Questions carry equal marks

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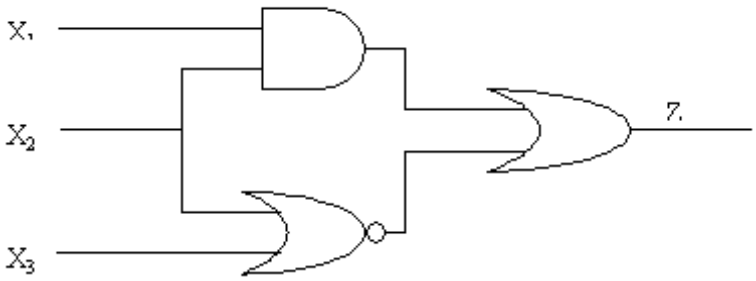
1. Derive the reliability function of a parallel ,series system compare the results with a fixed R(t) = 0.9 for each module used. [6+6+4]

2. (a) Illustrate the principles of path sensitizing method for the circuit given below and generate test vectors for different paths having different faults on them as shown in the figure1.



$Z = X_1X_2 + \overline{X}_2\overline{X}_3$

Figure 1:

   (b) How is path sensitization method advantageous over Fault Table method.Prove it for the above example. [8+8]

3. Derive the Reliability factor of TMR and Triplicathd TMR systems. Show that R(t) of Triplicated TMR is better than R(t) of TMR system. [5+5+6]

4. Explain the scheme proposed by lala for incorporating redundancy in the design of digital systems on single chip. [4+4+4+4]

5. (a) Design a checker for 1 out of 3 codes that satisfy the partially strongly fault secure properties.

   (b) Explain the principle of operation of strongly fault secure circuit with one example. [8+8]

6. Explain the steps to derive G-functions which generates the $C_i(o \leq i \leq m)$ check bits in modified Berger code specially for detecting uni-directional output errors in PLAs. Take an example to explain the above steps. [16]

7. (a) What are the goals of a design for testability?
   (b) What are the different DET methods available? Explain at least two such techniques. [6+4+6]

8. (a) Discuss the sequential circuit design using nonscan techniques.
   (b) i. What is meant by Enhanced controllability?
   ii. How is a sequential circuit modified for the above sequential circuit and enhanced controllability? [6+4+6]

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Code No: RR321503 **Set No. 3**

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FAULT TOLERANT SYSTEMS
(Computer Science & Systems Engineering)

Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
All Questions carry equal marks

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1. (a) If a system has 4000 identical components with a failure rate of 0.02% per 1000 hours. Find the MTBF of such a system.
   (b) Explain the phenomenon of Bath tub response for a Time Vs failure rate of a system. [8+8]
2. (a) Distinguish between fault detectionand fault location [2+2]
   (b) Illustrate the principles involved in fault table method of test generation using the figure1 given below.Verify the above test vector, generated, with the help of D-algorithm for C SAO fault. [12]

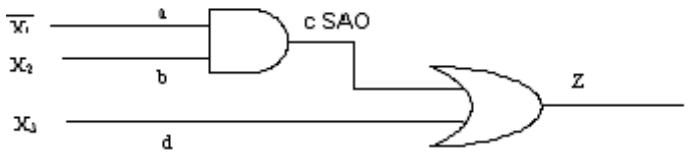

Figure 1:

3. (a) Distinguish between hybrid redundancy and triple modular redundancy and explain?
   (b) Realize hybrid redundancy with triple modular redundancy core. [5+5+6]
4. With an example explain :
   (a) software redundancy.
   (b) time redundancy. [8+8]
5. (a) Design a combinational self - testing checkers for k - out of 2 k codes, which are self-testing.
   (b) List out the importance and advantages of self - checking checker circuits. [8+8]
6. Design a sequential circuit using a partition theory for the given state table. [16]

PS	NS, I_1	I/P, I_2	Z I_3	I_4
A	C,0	C,0	A,0	A,0
B	B,1	C,0	D,1	A,0
C	C,0	B,0	A,0	A,0
D	B,1	A,0	D,1	A,0
E	E,0	E,0	A,0	A,0

7. Write a short notes an [4x4=16]
   (a) Controllability
   (b) Observability
   (c) Positive unate function
   (d) Syndrom relations of all types of terminating gates.
8. (a) What is meant by built in test of VLSI? Explain.
   (b) Discuss the crosscheck approach to incorporate test circuitry into the basic cells used in implement VLSI design. [8+8]

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Code No: RR321503 **Set No. 4**

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Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
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1. Explain the following with examples.
   (a) Bridging faults.
   (b) Stuck open fault.
   (c) Stuck at faults. [6+4+6]

2. (a) Illustrate the principles of path sensitizing method for the circuit given below and generate test vectors for different paths having different faults on them as shown in the figure1.

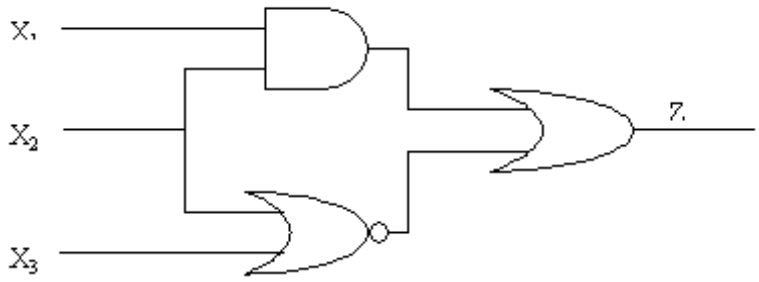

Figure 1:

   (b) How is path sensitization method advantageous over Fault Table method.Prove it for the above example. [8+8]

3. (a) Construct a seven-bit error correcting code to represent the decimal digit by augmenting the Excess-3 code and by using add-1 parity check.
   (b) Design a redundant circuit for $f = a \oplus b$ [9+7]

4. (a) Explain in detail the practicle fault Tolerant space shuttle computer complex system.
   (b) What are the different ways to have software redundancy. [8+8]

5. (a) Design a combinational self - testing checkers for k - out of 2 k codes, which are self-testing.

(b) List out the importance and advantages of self - checking checker circuits. [8+8]

6. Design a sequential circuit using a partition theory for the given state table. [16]

PS	NS, I_1	I/P, I_2	Z I_3	I_4
A	C,0	C,0	A,0	A,0
B	B,1	C,0	D,1	A,0
C	C,0	B,0	A,0	A,0
D	B,1	A,0	D,1	A,0
E	E,0	E,0	A,0	A,0

7. Explain the technique for designing minimally testable network which produces a circuit which can be tested by three tests only.Modify the function $f = \overline{A}\ \overline{B}$C +A $\overline{B}\ \overline{C}$ into a circuit which has only three tests. [10+6]

8. (a) What is meant by built in test of VLSI? Explain.

   (b) Discuss the crosscheck approach to incorporate test circuitry into the basic cells used in implement VLSI design. [8+8]

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