Code No: RR321301 **Set No. 1**

III B.Tech II Semester Supplementary Examinations,
November/December 2005
COMPUTER ORGANIZATION
(Electronics & Control Engineering)

Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
All Questions carry equal marks

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1. Explain the generic structure of IAS computer in detail with the help of a block diagram. [16]

2. (a) Explain about booth coding
   (b) Find the booth coded numbers of the following binary numbers
      i. 01101111101
      ii. 000111110110 [8+8]

3. Explain various power PC addressing modes with algorithms [16]

4. (a) Explain about the machine state register.
   (b) Discuss about the sequence of steps that occurs when an interrupt occurs [6+10]

5. (a) Differentiate between single versus two-level caches.
   (b) Elaborate on Pentium Cache Organization. [8+8]

6. Discuss the major functions and requirements for an I/O module. [16]

7. Discuss about horizontal and vertical instruction formats. Also differentiate between horizontal and vertical instruction formats. [16]

8. Assume that 20 percent of the instructions executed on a computer are branch instruction and delayed branching is used with one delay slot. Estimate the gain in performance if the complier is able to use 85 percent of the delay slots [16]

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Code No: RR321301 **Set No. 2**

III B.Tech II Semester Supplementary Examinations,
November/December 2005
COMPUTER ORGANIZATION
(Electronics & Control Engineering)

Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
All Questions carry equal marks

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1. (a) Draw and explain the timing of read operation in both synchronous and asynchronous timing.
   (b) Discuss various data transfer types supported by buses [8+8]
2. (a) Find the output binary number after performing the following arithmetic operations
      i. 111.01 + 10.111
      ii. 11.01 + 110.11
      iii. 110.11 - 111.01
   (b) Explain about the longhand division of binary integers. [6+10]
3. Discuss various key design issues of an instruction format. [16]
4. (a) List and describe different Motorola 88000 bit-field instructions.
   (b) Discuss about register management in Motorola 88000 [8+8]
5. (a) Explain any three replacement algorithms with examples.
   (b) Discuss in detail about set associative mapping in cache memory. [8+8]
6. Discuss about data organization and formatting of magnetic disk in detail [16]
7. (a) Differentiate between micro programmed and hard wired control units with merits and demerits of each.
   (b) Discuss about the design considerations of micro instruction sequencing technique. [8+8]
8. (a) Why special handling is required for branch instruction in a pipelined processor. Explain with examples.
   (b) How would you determine the number of pipeline stages in a pipelined processor [10+6]

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Code No: RR321301 **Set No. 3**

III B.Tech II Semester Supplementary Examinations,
November/December 2005
COMPUTER ORGANIZATION
(Electronics & Control Engineering)

Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
All Questions carry equal marks

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1. Explain about VonNeumann architecture design in detail. [16]

2. (a) Find the output binary number after performing the arithmatic operation using 1's complement representation.
   i. 111.01 + 10.111
   ii. 110.11 - 111.01
   (b) Explain steps involved in the addition of numbers using 2's complement notation. [10+6]

3. Explain various power PC addressing modes with algorithms [16]

4. (a) List and describe various co-processor and special instructions of MIPS R-series processors.
   (b) Differentiate between theoretical R3000 and actual R4000 super pipelines. [10+6]

5. (a) Explain any three replacement algorithms with examples.
   (b) Discuss in detail about set associative mapping in cache memory. [8+8]

6. (a) Explain how bus arbitration is done in DMA transfer
   (b) Discuss about the generic model of an I/O module. [8+8]

7. (a) On which types of information, a conditional branch instruction depends?
   (b) Explain about IBM 3033 control address register
   (c) Discuss about characteristics and terminology of microinstruction spectrum [5+5+6]

8. (a) Why special handling is required for branch instruction in a pipelined processor. Explain with examples.
   (b) How would you determine the number of pipeline stages in a pipelined processor [10+6]

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Code No: RR321301 **Set No. 4**

III B.Tech II Semester Supplementary Examinations,
November/December 2005
COMPUTER ORGANIZATION
(Electronics & Control Engineering)

Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
All Questions carry equal marks

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1. Explain the expanded structure of IAS computer with a neat block diagram. [16]
2. Explain about error detecting and correcting codes. What is their relevance [16]
3. Explain various power PC addressing modes with algorithms [16]
4. (a) List and describe integer arithmetic and logical instructions of Motorola 88000
   (b) Discuss about functioning of Motorola 88000 instruction unit pipeline. [8+8]
5. (a) What are the memory management requirements.
   (b) Elaborate on address translation in virtual memories [8+8]
6. (a) Explain about magnetic disk layout
   (b) Elaborate on Winchester disk track format. [8+8]
7. (a) Differentiate between horizontal and vertical micro instructions.
   (b) Discuss about functioning of micro-programmed control unit. [8+8]
8. (a) Explain different types of parallel processors.
   (b) What do you mean by compound instruction? Give examples
   (c) Elaborate on registers of the IBM3090 vector facility. [4+6+6]

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