Code No: RR320405 **Set No. 1**

III B.Tech II Semester Supplementary Examinations, November/December 2005
VLSI DESIGN
(Common to Electronics & Communication Engineering and Electronics & Telematics)

Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
All Questions carry equal marks

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1. (a) Clearly explain the body effect of the MOSFET.
   (b) Clearly explain about channel length modulation of the MOSFET. [8+8]
2. With neat sketches explain BICMOS fabrication in an n-well process. [16]
3. What is a stick diagram and explain about different symbols used for components in stick diagram. [16]
4. Design a layout diagram for CMOS inverter. [16]
5. Two nMOS inverters are cascaded to drive a capacitive load C_L=16Cg as shown in Figure 1. Calculate the pair delay Vin to Vout in terms of τ for the given data.

   Inverter -A

   $L_{P.U}$= 16λ , $W_{P.U}$ = 2 λ , $L_{P.d}$ = 2 λ , $W_{P.d}$ = 2 λ

   Inverter -B

   $L_{P.U}$= 2λ , $W_{P.U}$ = 2 λ , $L_{P.d}$ = 2 λ , $W_{P.d}$ = 8 λ [16]

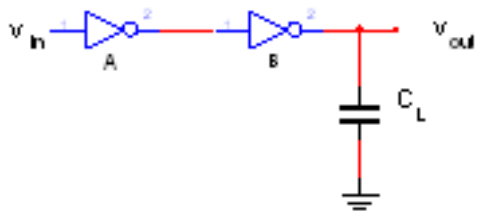

Figure 1:

6. Using PLA Implement Half-adder circuit. [16]
7. Explain the following processes in the ASIC design flow.
   (a) Post - layout timing simulation.
   (b) Post synthesis simulation. [8+8]
8. With neat sketches explain the electron lithography process. [16]

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Code No: RR320405 **Set No. 2**

III B.Tech II Semester Supplementary Examinations,
November/December 2005
VLSI DESIGN
(Common to Electronics & Communication Engineering and Electronics & Telematics)

Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
All Questions carry equal marks

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1. (a) Find g_m and r_{ds} for an n-channel transistor with
   V_{GS} = 1.2V; Vtn = 0.8V; W/L = 10; μnCox = 92 μA/V^{2}and V_{DS} = Veff + 0.5V
   The out put impedance constant. $\lambda = 95.3 \times 10^{-3}$ V^{-1}
   (b) Explain the term Figure of merit of a MOS Transistor. [10+6]

2. (a) Compare between CMOS an bipolar technologies.
   (b) With neat sketches explain nMOS fabrication process. [8+8]

3. Design a stick diagram for p-MOS Ex-OR gate. [16]

4. Explain with suitable examples how design the layout of a gate to maximize performance and minimize area. [16]

5. Calculate on resistance of the circuit shown in Figure 1 from V_{DD} to GND. If n-channel sheet resistance Rsn = 10 ^{4} Ω per square and p-channel sheet resistance $Rsp = 3.5 \times 10^4\Omega$ per square. [16]

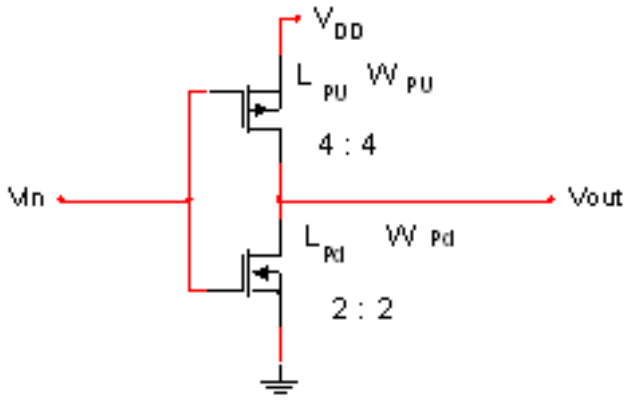

Figure 1:

6. With neat sketches explain the architecture of PAL. [16]

7. (a) Define the term DFT and explain about it.
   (b) Explain any one test procedure to test sequential logic. [8+8]

8. Mention different growth technologies of the thin oxides and explain about any one technique. [16]

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Code No: RR320405 **Set No. 3**

III B.Tech II Semester Supplementary Examinations,
November/December 2005
VLSI DESIGN
(Common to Electronics & Communication Engineering and Electronics & Telematics)

Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
All Questions carry equal marks

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1. (a) Drive an equation for R_{DS} of an n-channel enhancement MOSFET in linear region.
   (b) For the Figure 1 shown, plot the trans conductance as a function of V_{DS}

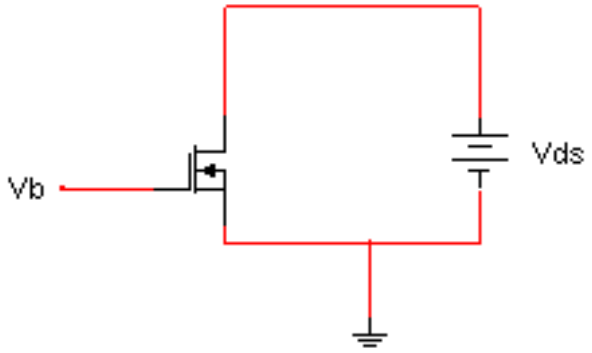

Figure 1:

[10+6]

2. (a) Compare between CMOS an bipolar technologies.
   (b) With neat sketches explain nMOS fabrication process. [8+8]

3. Design a stick diagram for the CMOS logic shown below $Y = \overline{(A+B).C}$ [16]

4. Design a layout diagram for nMOS inverter. [16]

5. Calculate the gate capacitance value of $5\mu m$ technology minimum sized transistor with gate to channel capacitance value is $4 \times 10^{-4} pF/\mu m^2$. [16]

6. Implement 4-2 Encoder using PROM. [16]

7. What are the different report files that are provided by the place and route tool and discuss clearly about each report file. [16]

8. Explain about the following Die bandings.
   (a) Eutectic die bonding.
   (b) Epoxy die bonding. [8+8]

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Code No: RR320405 **Set No. 4**

III B.Tech II Semester Supplementary Examinations, November/December 2005
VLSI DESIGN
(Common to Electronics & Communication Engineering and Electronics & Telematics)

Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
All Questions carry equal marks

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1. (a) Explain with neat sketches the Drain and Transfer characteristics of n-channel enhancement MOSFET.
   (b) With neat sketches explain the transfer characteristics of a CMOS inverter. [10+6]
2. With neat sketches explain how Diodes and Resistors are fabricated in pMOS process. [16]
3. What is a stick diagram and explain about different symbols used for components in stick diagram. [16]
4. Design a layout diagram for the CMOS logic shown below $Y = \overline{(A + B + C)}$ [16]
5. Two nMOS inverters are cascaded to drive a capacitive load C_L=14Cg as shown in Figure 1. Calculate the pair delay Vin to Vout in terms of τ for the given data.

   Inverter -A

   $L_{P.U}$= 12λ , $W_{P.U}$ = 4 λ , $L_{P.d}$ = 1 λ , $W_{P.d}$ = 1 λ

   Inverter -B

   $L_{P.U}$= 4λ , $W_{P.U}$ = 4 λ , $L_{P.d}$ = 2 λ , $W_{P.d}$ = 8 λ [16]

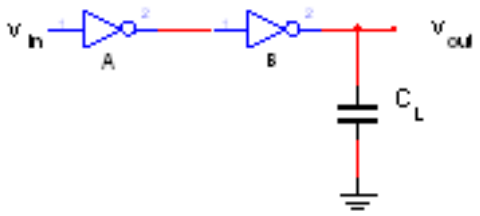

Figure 1:

6. Explain about the following gate array based ASICS
   (a) Channel gate arrays
   (b) Channel less gate arrays
   (c) Structured gate arrays [5+5+6]

7. What are the inputs that are provided to the synthesis tool? And explain completely about synthesis process in the ASIC design. [16]

8. With neat sketches explain the oxidation process in the IC fabrication process. [16]

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