Code No: RR320202 **Set No. 1**

III B.Tech II Semester Supplementary Examinations, November/December 2005
MICROPROCESSORS AND INTERFACING
(Common to Electrical & Electronic Engineering, Electronics & Communication Engineering, Electronics & Instrumentation Engineering, Bio-Medical Engineering, Electronics & Control Engineering and Electronics & Telematics)

Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
All Questions carry equal marks

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1. Explain the difference between memory page and memory segmentation? What are the minimum number of segments that are necessary to provide segmentation concept? Explain why segmentation is useful in real-time applications? [16]

2. (a) Using DF flag and string instructions, write an assembly language program to move a block of data of length N from source to destination. Assume all possible conditions.
   (b) Discuss the importance of procedures in assembly language programming? [10+6]

3. Describe the function of the following pins in 8086 maximum mode of operation.
   (a) $\overline{TEST}$
   (b) RQ/GT_0 and RQ/GT_1
   (c) QS_0 & QS_1
   (d) S_0, S_1 , S_2 [2+4+4+6]

4. Interface a 12-bit DAC to 8255 with an address map of 0C00H to 0C03H. The DAC provides output in the range of +5V to -5V. Write the instruction sequence.
   (a) For generating a square wave with a peak to peak voltage of 4V and the frequency will be selected from memory location 'F'.
   (b) For generating a triangular wave with a maximum voltage of +3V and a minimum of -2V. [6+10]

5. (a) Explain demand transfer mode and block transfer mode of 8237?
   (b) Show how 8237's are cascaded to provide more number of DRQ's and explain the operation?
   (c) Explain how memory to memory transfer is performed with 8237? [5+6+5]

6. (a) What is the purpose of operational command words of 8259? Explain their format and the use?

(b) What is type 2 interrupt? Explain the condition for initiating type 2 interrupt? What is the priority of this interrupt in 8086? [10+6]

7. (a) With a sketch explain 74LS138 decoder and its use?

   (b) Generate chip select signals with the help of 74LS138 to six memory chips of size 16KB, with the address map from 00000H to 17FFFH? [6+10]

8. (a) Explain the alternate functions of Port 0, Port 2 and Port 3?

   (b) Discuss the interrupt structure of 8051? Mention the priority? Explain how least priority is made as highest priority? [9+7]

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Code No: RR320202 **Set No. 2**

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Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
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1. Discuss the general functions of all general-purpose resisters of 8086? Explain the special function of each resister and instruction support for these functions. [16]

2. (a) What is a recursive procedure? Write a recursive procedure to calculate the factorial of number N, where N is a two-digit Hex number?
   (b) What are the loop instructions of 8086? Explain the use of DF flag in the execution of string instructions. [9+7]

3. (a) What are the control signals useful for inter processor communication using 8086? What instruction set support is provided in 8086?
   (b) Design an I/O port decoder that generate the following low-bank I/O strobes: 0010H, 0020H, 0030H, 0040H. [6+10]

4. Interface an 8-bit DAC to 8255 with an address map of 0100H to 0103H. The DAC provides output in the range of +5V to -5V. Write the instruction sequence for the following?
   (a) For generating a square wave with a peak to peak voltage of 2V and the frequency will be selected from memory location 'FREQ'. [6+10]
   (b) For generating a triangular wave with a maximum voltage of +4V and a minimum of -2V.

5. Explain with a neat sketch all registers of 8237 and their use in DMA transfer?[16]

6. With detailed hardware and the associated algorithm, explain how a real time clock will be implemented in an 8086 based system. [16]

7. A target system based on 8088 processor uses less amount of SRAM. The programs are stored in EPROM that starts from F0000H ends with the address of FFFFFH. The capacity of SRAM is 8KB interfaced at address 00000H. The chip size is 8KB for EPROM and SRAM. Show the complete memory interface? [16]

8. (a) Draw and discuss the formats and bit definitions of the following SFRs in 8051 microcontroller?
      i. SCON

ii. TCON [4x2=8]

(b) Discuss the following signal descriptions?

i. ALE/PROG
ii. $\overline{EA}/V_{pp}$
iii. $\overline{PSEN}$
iv. RXD [2x4=8]

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Code No: RR320202 **Set No. 3**

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Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
All Questions carry equal marks

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1. (a) Explain why 8086 internal architecture is divided into BIU and EU? Discuss the A-bus, B-bus and C-bus and their use?
   (b) Explain the difference between memory segmentation and memory page? Why segmentation is useful in real-time applications? [8+8]
2. (a) Develop a far procedure declared as PUBLIC to convert a 4-digit BCD number to its equivalent hex number?
   (b) Develop a near procedure to find the GCD of two numbers of 2-digit Hex. Use this procedure to find the GCD of three numbers? [8+8]
3. (a) What is the purpose of ALE, BHE, DT/$\overline{R}$ and $\overline{DEN}$ pins of 8086? Show their timing in the system bus cycle of 8086?
   (b) Why 8086 memory is mapped into 2 byte wide banks? What logic levels are found with BHE and A0 when 8086 reads a word from the address 0A0AH? [10+6]
4. Explain why 8255 ports are divided into two groups? Discuss how these groups are controlled in different modes of operation? Explain different control signals and their associated pins for bi-directional I/O mode of operation? [4+6+6]
5. (a) Explain demand transfer mode and block transfer mode of 8237?
   (b) Show how 8237's are cascaded to provide more number of DRQ's and explain the operation?
   (c) Explain how memory to memory transfer is performed with 8237? [5+6+5]
6. Write an initialization sequence for an 8259 that is the only 8259 in an 8086 based system, with an even address of 0F0H that will cause.
   (a) Request to the edge triggered mode
   (b) IR_0 request to an interrupt type 30
   (c) SP/EN to output a disable signal to the data-bus transceivers.
   (d) The ISR bits to be cleared automatically at the end of second INTA pulse.

(e) The IMR to be cleared.

(f) The highest priority interrupt will be IR_6. [16]

7. (a) Discuss the organization of FLASH memory? Explain the FLASH memory command definitions?

(b) With the help of basic cell explain SRAM and DRAM? Discuss the advantages and disadvantages of the above memories? [6+10]

8. (a) Discuss the register set of MCS-51 family of microcontrollers?

(b) Explain the alternate functions of Port 0, Port 2 and Port 3? [8+8]

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Code No: RR320202 **Set No. 4**

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Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
All Questions carry equal marks

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1. (a) Discuss the general functions of all general-purpose resisters of 8086? Explain the special function of each resister and instruction support for these functions.
   (b) What is the use of segmentation? Discuss one application area? Explain how segmentation provides efficient task switching mechanism? [10+6]

2. (a) Give the assembly language implementation of the following.
      i. DO WHILE
      ii. FOR [4+4]
   (b) What is a recursive procedure? Write a recursive procedure to calculate the factorial of number N, where N is a two-digit Hex number? [8]

3. Distinguish between a memory read and write machine cycle? Draw the timing diagrams in minimum and maximum modes of operation? [8+8]

4. Write the necessary instruction sequence to initialize 8255 with address 0C00H to 0C03H for the following combinations.
   (a) Port A as input port in mode 1 and port B as input port in mode 1 without the interrupt driven i/o.
   (b) Port A in mode 2 as output port and port B as input port in mode 0 with interrupt driven i/o.
   (c) Port A in mode 0, port c upper half as input ports and port B as input port in mode 1 with interrupt driven i/o.
   (d) Port A as output port in mode 1 with active interrupt, port B as input port in mode 0 and port C lower half as output port in mode 0. [4 x 4 =16]

5. (a) Explain demand transfer mode and block transfer mode of 8237?
   (b) Show how 8237's are cascaded to provide more number of DRQ's and explain the operation?
   (c) Explain how memory to memory transfer is performed with 8237? [5+6+5]

6. (a) Draw the block diagram of 8259 and explain each block?

(b) Explain how IRET instruction is executed? [12+4]

7. In an SDK-86 kit 128KB SRAM and 64KB EPROM is provided on system and provision for expansion of another 128KB SRAM is given. The on system SRAM address starts from 00000H and that of EPROM ends with FFFFFH. The expansion slot address map is from 80000H to 9FFFFH. The size of SRAM chip is 64KB. EPROM chip size is 16KB. Give the complete memory interface and also the address map for individual chips? [16]

8. An 8051 based system requires external memory of four 8Kbytes of SRAM each and two chips of EPROM of size 4Kbytes. The EPROM starts at address 1000H. SRAM address map follows EPROM map. Give the complete memory interface?

[16]

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