Code No: NR320404 **NR**

III B.Tech II Semester Supplementary Examinations, November/December 2005
VLSI TECHNOLOGY
(Common to Electronics & Communication Engineering and Electronics & Telematics)

Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
All Questions carry equal marks

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1. (a) Trace the evolution of IC technology starting from discrete bipolar transistors to VLSI. Highlight various stages of evolution chronologically.
   (b) Explain the terms SSI, LSI, VLSI and ULSI with reference to feature size, number of transistors per chip and applications. [8+8]
2. (a) Explain the functioning of a MOS pass transistor.
   (b) Determine the pull up to pull down ratio of an n MOS inverter when driven through one or more pass transistors. [6+10]
3. Write notes on:
   (a) FPGAs
   (b) PLAs
   (c) PLDs [16]
4. Explain about the design approaches for full custom and semi custom Devices [16]
5. Briefly explain the following verification tools:
   (a) timing verifiers
   (b) design rule checkers
   (c) layout extractions and
   (d) test vectors. [4+4+4+4]
6. Explain the following synthesis methods w.r.t VLSI chip design.
   (a) Behavioral level [4]
   (b) RTL level [3]
   (c) Logic level [3]
   (d) structural level [3]
   (e) layout level [3]
7. (a) How packaging is affects on the performance of VLSI chip?
   (b) Explain surface mounting type packages. [8+8]

8. (a) Prove that the combination of BJT and MOS technology offers the best performance in Analog VLSI design.
   (b) Draw the block diagram of D/A converter suitable for VLSI Analog Circuits and explain. [8+8]

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