Code No: RR320501 **Set No. 1**

III B.Tech II Semester Supplementary Examinations,
November/December 2005
ADVANCED COMPUTER ARCHITECTURE
(Common to Computer Science & Engineering, Information Technology and Computer Science & Systems Engineering)

Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
All Questions carry equal marks

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1. Explain different parallel processing mechanisms that are possible in uniprocessor computersl. [16]

2. (a) Describe the effect of conditional statements on pipeline processes Suggest improvements.
   (b) Explain how Data Buffering and Busing Structures improves efficiency of pipeline processors. [8+8]

3. (a) Classify the various multistage SIMD interconnection N/W according to the 3 distinct features blocking , rearrangeable and non-blocking
   (b) The Omega N/W is capable of performing broadcasting. .If the number of destination $PE's$ is a power of two , give a simple routing algorithm to achieve this capability [8+8]

4. (a) What is an associative memory? Discuss a simple associative memory organization with suitable diagrams.
   (b) Explain the architecture of PEPE association processor [8+8]

5. (a) Explain briefly the communication between processors in a Multiprocessor environment.
   (b) With suitable diagram, explain loosely coupled and tightly coupled Multiprocessors. [6+10]

6. (a) Explain the L-M memory organization for a multiprocessor system, with the help of a diagram.
   (b) Describe language features that can exploit parallelism in multiprocessor environment. [8+8]

7. (a) Explain briefly, the architecture of the Irvine data flow computer.
   (b) Explain the concept of grouping instruction cells into cellblocks. [8+8]

8. (a) Give the features of Hydra operating system.
   (b) Demonstrate the effect of memory contention on the performance of C.mmp. [8+8]

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Code No: RR320501 **Set No. 2**

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Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
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1. (a) Describe the various parallel computer structures in common use and differentiate among them.
   (b) Distinguish between
      i. temporal parallelism
      ii. Spatial parallelism
      iii. asynchronous parallelism. Illustrate each of these with examples. [8+8]
2. (a) What is Internal Forwarding? Explain different techniques.
   (b) Explain different data dependant hazards and how these hazards have to be handled so for effective Processing. [8+8]
3. (a) Explain the connectivity of Illiac Network with N = 16
   (b) Draw a neat 16*16 baseline network and Explain its connectivity between its nodes. [8+8]
4. (a) Describe M(j,k) sorting algorithm.
   (b) Describe a Bit serial Associative memory organization with suitable diagram [8+8]
5. (a) Explain briefly the steps involved in a cross-cluster memory access.
   (b) Explain the model of a tightly coupled Multiprocessor system without private cache [8+8]
6. (a) Explain the L-M memory organization for a multiprocessor system, with the help of a diagram.
   (b) Describe language features that can exploit parallelism in multiprocessor environment. [8+8]
7. (a) Compare data driven and dependence driven computing models.
   (b) Explain the multilevel program abstraction in the event driven data flow computing model. [8+8]
8. (a) What are the fundamental classes of performance measures? Explain in detail
   (b) Discuss in detail the performance of M/M/1 queuing structure. [8+8]

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Code No: RR320501 **Set No. 3**

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Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
All Questions carry equal marks

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1. What is the conceptual meaning of computer Architecture? Explain different computer architectural classification schemes in detail. [16]

2. (a) How the vector length effects the processing efficiency ? Explain different enhancement techniques.
   (b) Describe memory interleaving mechanisms. [8+8]

3. (a) What is the speed up of a Barrel Shifter over Illiac network . Explain.
   (b) Name some data manipulating functions and describe the primitive operations that can be performed using these functions. [8+8]

4. (a) What is an associative memory? Discuss a simple associative memory organization with suitable diagrams.
   (b) Explain the architecture of PEPE association processor [8+8]

5. (a) Explain briefly the steps involved in a cross-cluster memory access.
   (b) Explain the model of a tightly coupled Multiprocessor system without private cache [8+8]

6. Briefly characterize the multicache cohenence problem and describe various methods that can be used to cope with the problem. [16]

7. (a) Describe any four systolic array configurations.
   (b) Describe how algorithms are mapped into VLSI arrays. [8+8]

8. (a) Draw and explain the dataflow and transfer rates in Cray X-MP with suitable diagram
   (b) Explain the vector computations on X-MP for the example: A = B+S*D. [8+8]

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Code No: RR320501 **Set No. 4**

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Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
All Questions carry equal marks

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1. (a) Consider three interleaved memory organizations for a main memory system containing 8 memory modules, M_0, M_1..., M_7. Each module has a capacity of 2K word. In total, the memory capacity is 16K words. The maximum memory bandwidth is 8 words /cycle. In each of the following organizations, first specify the memory address format (14 bits), then show the address assignment patterns in each memory module, and finally indicate the maximum bandwidth when one of the 8 modules fails to function. Comment on the relative merits of the three interleaved memory organizations.
   i. Eight-way interleaved memory organization (one group)
   ii. Grouped four-way interleaved memory organization (two groups).
   iii. Grouped two-way interleaved memory organization (four groups)

   (b) Give the advantages and disadvantages of the three interleaved memory organizations, S-access, C-access and the C/S access on the basis of memory bandwidth, storage schemes used, access conflict resolution and cost-effectiveness trade offs. [8+8]

2. (a) Derive the expressions for efficiency, throughput and speed up for k stage pipeline for n tasks.

   (b) What are key issues in the design of an efficient dynamic pipeline processor. [8+8]

3. (a) What is the speed up of a Barrel Shifter over Illiac network . Explain.

   (b) Name some data manipulating functions and describe the primitive operations that can be performed using these functions. [8+8]

4. (a) Explain the implementation of SIMD fast Fourier Transform.

   (b) Explain on the connection issues in while using SIMD inter connection networks. [8+8]

5. (a) With the help of diagrams, the working of tightly coupled Multiprocessors without private cache. What is the advantage of using Private cache?

   (b) Describe the desirable characteristics of a processor to be effective in a multiprocessor environment. [8+8]

6. (a) Explain performance tradeoffs in memory organizations.

(b) How caches can be associated with shared memory? How this configuration avoids cache coherence. [8+8]

7. (a) Explain the functional structure of the processing element(PE) in Arvind's data Flow machine.

   (b) Describe switches, arbiters and distributers used in Data flow network construction. [8+8]

8. (a) Describe the criteria for evaluation of computer systems. Give their importance.

   (b) Describe a Stochastic model of a computer system that can used for evaluation. [8+8]

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