Code No: RR411403 **Set No.1**

IV B.Tech. I Semester Regular Examinations, November -2005
COMPUTER ORGANISATION
(Mechatronics)

Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
All Questions carry equal marks

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1. (a) Under what conditions do the following over flow / under flow conditions occur in floating point arithmetic.
   i. Fraction overflow
   ii. Fraction underflow
   iii. Exponent overflow
   iv. Exponent underflow

   (b) Why is dividend alignment carried out in floating point division. [10+6]

2. (a) A CPU has 16 registers, an ALU with 16 logic and 16 arithmetic operations and a shift register with 8 operations all connected on a common bus.
   i. Formulate a control word to specify the various micro-operations for the CPU with the number of bits in a general encoding scheme for each field.
   ii. Show the bits of a control word that specifies the operation $R_7 \leftarrow R_1 + R_{14}$

   (b) Under what conditions would it be more feasible to use a hard-wired control than a microprogrammed control. [12+4]

3. (a) The fetch and decode phase of an instruction cycle can be specified by the following register transfer statements:

$$\begin{aligned} T_0 &: \quad AR \leftarrow PC \\ T_1 &: \quad IR \leftarrow M(AR), PC \leftarrow PC + 1 \\ T_2 &: \quad D_{0-7} \leftarrow Decode\, IR\ (12-14), AR \leftarrow IR(0-11) \\ & \qquad\qquad I \leftarrow IR(15) \end{aligned}$$

   Draw the schematic diagram of the bus system that can perform the above register transfer operations and explain how they are performed.

   (b) Using 4 full adders, realize an arithmetic unit which can perform addition, substraction, increment and decrement micro-operations. Specify in tabular form the micro-control signals to be applied to it to perform these micro operations. [8+8]

4. (a) Convert the numerical arithmatic expression

   (4 + 5)[7*{ (8 + 4) 3}]

   into reverse polish notation (RPN). Explain how a stack can be used in a computer to evaluate the expression and show the stack operations for evaluating the numerical result.

   (b) Give the schematic diagram of a micro-programmed control unit and explain the function of its different components. [8+8]

5. Write short notes on the following mapping processes of a cache memory
   (a) Associative mapping
   (b) Direct-mapping
   (c) Set Associative mapping [5+5+6]
6. (a) Relate the address space and memory space in a virtual memory system.
   (b) Explain the address mapping in virtual memory using pages. [8+8]
7. (a) What is the difference between internal and external interrupts?
   (b) What is the difference between a software interrupt and a sub-routine call?
   (c) What advantages does interrupt based I/O have over polled I/O? Under what condition is it not feasible to use polled I/O? [5+5+6]
8. Explain the following:
   (a) Vertical Programming
   (b) Bit-slice Processors
   (c) IOP
   (d) DMA [4×4]

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Code No: RR411403 **Set No.2**

IV B.Tech. I Semester Regular Examinations, November -2005
COMPUTER ORGANISATION
(Mechatronics)

Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
All Questions carry equal marks

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1. (a) What are various division algorithms available for the binary division?
   (b) Explain with a flow chart the divide operation of signed magnitude numbers. Provide necessary hardware configuration. [8+8]
2. (a) What are different characteristics of RISC architecture.
   (b) What is pipelining?
   (c) Explain the concept of overlapped register windows. [6+4+6]
3. (a) Discuss different addressing modes with necessary examples.
   (b) Give five examples of external and internal interrupts. [8+8]
4. (a) Write an ALP (for 8085 CPU) for arranging the given 255 bytes in ascending order. Assume data.
   (b) Draw the timing diagram for the instruction "LDA address". [8+8]
5. (a) Draw the block diagram of micro programmed control organization.
   (b) Explain the selection of address for control memory. [8+8]
6. (a) What are salient features of cache memory?
   (b) Write short notes on
      i. Associative mapping
      ii. Direct mapping
      iii. Set associative mapping. [4+12]
7. (a) Give the block diagram of a computer with IOP and explain different forms of communication between CPU and IOP with a flow chart.
   (b) Why does DMA have priority over the CPU when both request a memory transfer? [10+6]
8. (a) Introduce Daisy-chain priority interrupt scheme with a block diagram.
   (b) Design a parallel priority interrupt hardware for a system with interrupt sources. [8+8]

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Code No: RR411403 **Set No.3**

IV B.Tech. I Semester Regular Examinations, November -2005
COMPUTER ORGANISATION
(Mechatronics)

Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
All Questions carry equal marks

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1. (a) Convert the following Numbers which are in base 9 into binary and perform the arithmetic operations?
$(78)_9+(24)_9-(68)_9$
   (b) Perform the following operation in Hexa decimal
      i. $(ABC9)_{16}+(2BDE)_{16}=(\quad)_{16}$
      ii. $(ABD)_{16}$ - $(CF)_{16}$
   (c) Perform the multiplication and division on base 4 numbers and give the results in base 4
      i. $(23)_4*(64)_{10}$
      ii. $(1231)_4 \div (64)_{10}$ [4+6+6]

2. (a) Describe any three instruction Formats?
   (b) Assume the capacity of Main Memory is 32 k*8 and there are 200 instructions, with 16 general purpose registers. Give the size of instruction with its format, where the instruction contains the OP code, the direct address, and the address of the next instruction as 3-fields. Give the size of the other instruction where the first two fields are same as above and 3^{rd} Field consists of Register. [8+8]

3. (a) Describe any 3-addressing modes?
   (b) Describe the concept of instruction Pipeline? [8+8]

4. Describe 8085 Microprocessor - Pin diagram and explain about each pin? [16]

5. Describe a Micro Program control unit with its block diagram? Compare vertical and Horizontal Micro instructions? [16]

6. (a) Describe the Cache Memory organization?
   (b) Compare SRAM and DRAM and describe them? [8+8]

7. (a) Describe the function of DMA with it's block diagram?
   (b) Describe interrupt driven I/O concept? [10+6]

8. Write short noteson any three of the following:
   (a) Virtual Memory
   (b) Nano Programming
   (c) RISC Processors

(d) I/O Processors [4×4]

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Code No: RR411403 **Set No.4**

IV B.Tech. I Semester Regular Examinations, November -2005
COMPUTER ORGANISATION
(Mechatronics)

Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
All Questions carry equal marks

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1. (a) Explain in detail the addition and substraction of floating point numbers with the help of a block diagram.
   (b) Design a hardware scheme for BCD adder. [8+8]
2. (a) What are various addressing modes? Explain with suitable examples.
   (b) How are the interrupts (S/W & H/W) organised in 8085 CPU. [8+8]
3. (a) Define the following:
      i. Micro Instruction
      ii. Micro Operation
      iii. Micro Program
      iv. Macro
   (b) What are different characteristics of RISC architecture.
   (c) Discuss pipelining. [6+5+5]
4. (a) Draw the block diagram of a micro program sequencer for a control memory and explain.
   (b) What are the differences between hardwired control and microprogrammed control? [8+8]
5. (a) Draw the pin diagram of 8085 CPU and discuss the function of each pin.
   (b) Write an ALP for arranging the given bytes in descending order. Assume data. [8+8]
6. Write short notes on:
   (a) Cache Memory
   (b) Virtual Memory [8+8]
7. (a) Introduce a Daisy-chain priority Interrupt scheme with a block diagram.
   (b) Explain the communication between a CPU and IOP with a neat flow chart. [8+8]
8. (a) Draw the block diagram of a DMA controller and explain the data transfer using DMA in a computer system.

(b) Why are the read and write control lines in a DMA controller bidirectional? Under what condition and what purpose are they used as inputs and outputs. [10+6]

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