Code No: RR411106 **Set No. 1**

IV B.Tech I Semester Regular Examinations, November 2005
VLSI DESIGN
(Bio-Medical Engineering)

Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
All Questions carry equal marks

⋆ ⋆ ⋆ ⋆ ⋆

1. A MOS Transistor in the active region measured to have a drain current of 20 μA when V_{DS}=Veff. When V_{DS} is increased by 0.5V, I_D increases to 23 μA. Estimate the out impedance r_{ds}, and the out impedance constant λ. [16]

2. (a) With neat sketches explain CMOS fabrication using p-well process.
   (b) With neat sketches explain pMOS fabrication process. [10+6]

3. What is a stick diagram and explain about different symbols used for components in stick diagram. [16]

4. Explain with suitable examples how design the layout of a gate to maximize performance and minimize area. [16]

5. Derive equations for rise time and fall time estimation of CMOS inverter circuit. [16]

6. With neat sketch clearly explain the architecture of a PLA. [16]

7. What are the inputs that are provided to the synthesis tool? And explain completely about synthesis process in the ASIC design. [16]

8. Explain about the following Die bandings.
   (a) Eutectic die bonding.
   (b) Epoxy die bonding. [8+8]

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Code No: RR411106 **Set No. 2**

IV B.Tech I Semester Regular Examinations, November 2005
VLSI DESIGN
(Bio-Medical Engineering)

Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
All Questions carry equal marks

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1. (a) Find g_m and r_{ds} for an n-channel transistor with
$V_{GS} = 1.2V$; Vtn = 0.8V; W/L = 10; μnCox = $92\mu A/V^2$and V_{DS} = Veff.
The out put impedance constant. $\lambda = 95.3 \times 10^{-3}V^{-1}$
(b) Define the term Threshold voltage of MOSFET and explain its significance. [10+6]

2. With neat sketches explain BICMOS fabrication in an n-well process. [16]

3. Design a stick diagram for two input CMOS NAND and NOR gates. [16]

4. Explain with suitable examples how design the layout of a gate to maximize performance and minimize area. [16]

5. Calculate on resistance of the circuit shown in Figure 1 from V_{DD} to GND. If n-channel sheet resistance Rsn = 10^{4} Ω per square and p-channel sheet resistance $Rsp = 1.5 \times 10^4\Omega$ per square. [16]

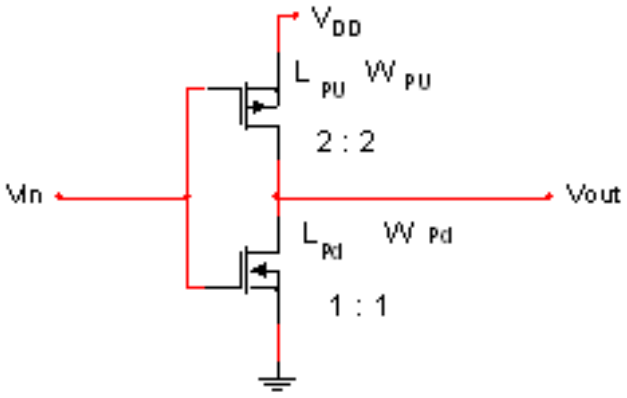

Figure 1:

6. With neat sketch explain clearly the architecture of the PROM. [16]

7. Clearly explain each step of high level design flow of an ASIC. [16]

8. Explain about the following Die bandings.
(a) Eutectic die bonding.

(b) Epoxy die bonding. [8+8]

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Code No: RR411106 **Set No. 3**

IV B.Tech I Semester Regular Examinations, November 2005
VLSI DESIGN
(Bio-Medical Engineering)

Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
All Questions carry equal marks

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1. A MOS Transistor in the active region measured to have a drain current of 20 μA when V_{DS}=Veff. When V_{DS} is increased by 0.5V, I_D increases to 23 μA. Estimate the out impedance r_{ds}, and the out impedance constant λ. [16]

2. (a) Compare between CMOS an bipolar technologies.
   (b) With neat sketches explain nMOS fabrication process. [8+8]

3. Design a stick diagram for the NMOS logic shown below $Y = \overline{(A+B).C}$ [16]

4. Design a layout diagram for pMOS inverter. [16]

5. Calculate on resistance of the circuit shown in Figure 1 from V_{DD} to GND. If n-channel sheet resistance Rsn = 10^4 Ω per square and p-channel sheet resistance $Rsp = 4.5 \times 10^4 \Omega$ per square. [16]

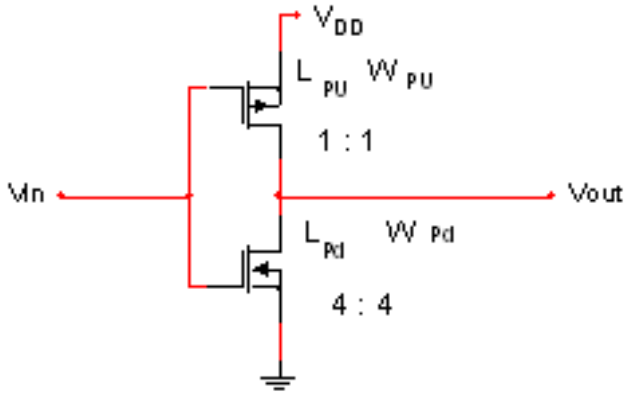

Figure 1:

6. Implement 4-2 Encoder using PROM. [16]

7. Mention about various types of simulators used in ASIC design flow and clearly discuss about the significance of each simulator. [16]

8. With neat sketches explain Atmospheric- pressure chemical vapor deposition method. [16]

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Code No: RR411106 **Set No. 4**

IV B.Tech I Semester Regular Examinations, November 2005
VLSI DESIGN
(Bio-Medical Engineering)

Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
All Questions carry equal marks

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1. (a) With neat sketches explain the formation of the inversion layer in P-channel Enhancement MOSFET.
   (b) An NMOS Transistor is operated in the triode region with the following parameters $V_{GS} = 4V$; $V_{tn} = 1V$; $V_{DS} = 2V$; $W/L = 100$; $\mu nCox = 90\ A/V^2$ Find its drain current and drain source resistance. [8+8]
2. With neat sketches explain how Diodes and Resistors are fabricated in pMOS process. [16]
3. Design a stick diagram for n-MOS Ex-NOR gate. [16]
4. Design a layout diagram for two input CMOS NAND gate. [16]
5. Calculate the gate capacitance value of $2\mu m$ technology minimum size transistor with gate to channel capacitance value is $8 \times 10^{-4} pF/\mu m^2$. [16]
6. (a) What are the advantages and disadvantages of the reconfiguration.
   (b) Mention different advantages of Anti fuse Technology. [8+8]
7. Name different layout analysis and design tools? Explain the job of these tools. [16]
8. With neat sketches explain Atmospheric- pressure chemical vapor deposition method. [16]

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