Code No: RR410408 **Set No.1**

IV B.Tech. I Semester Regular Examinations, November -2005
ADVANCED COMPUTER ARCHITECTURE
(Common to Electronics & Communication Engineering and Electronics & Computer Engineering)

Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
All Questions carry equal marks

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1. (a) Explain the requirement of large scale computations in substantiate the use of Numerical weather forecasting and large scale computation in Socio economics and Government use.
   (b) Explain the significance and necessity of Super computers in Engineering Design and Automation. [8+8]
2. (a) Explain the operational principles of pipeline computation using a pipelined floating-point adder as an example.
   (b) Describe the concepts of efficiency and throughput as applicable to a linear pipeline. [8+8]
3. Discuss the various the Multistage interconnection networks and give their importance and relative merits. [16]
4. Describe a student − file search in a bit parallel associative memory- Assume relevant data. [16]
5. (a) Give the computer module of a nonhierarchical loosely coupled multiprocessor system.
   (b) Give the various components of the Kmap in Cm*, architecture and explain the message transfer mechanism between modules. [10+6]
6. (a) Describe multicache problems? Describe methods to solve these problems.
   (b) Describe a methodology to evaluate different multiprocessor memory configurations. [8+8]
7. (a) Explain briefly, the architecture of the Irvine data flow computer.
   (b) Explain the concept of grouping instruction cells into cellblocks. [8+8]
8. (a) Draw and explain the dataflow and transfer rates in Cray X-MP with suitable diagram
   (b) Explain the vector computations on X-MP for the example: A = B+S*D. [8+8]

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Code No: RR410408 **Set No.2**

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Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
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1. (a) Differentiate between Multiprogramming and Time sharing.
   (b) What is Balancing of sub system Bandwidth.? How does it help to improve processing speed. [8+8]
2. (a) Describe the various issues and design principles of pipelines instruction units.
   (b) What are carry − save adders? Design a pipeline multiplication scheme using the carry-save adders. [8+8]
3. Discuss the working of Shuffle Exchange recirculating network and how Omega network is derived from this, for 8 nodes. [16]
4. (a) How is the Summation functionality performed in a SIMD Machine
   (b) Name some SIMD parallel algorithms and along with their complevity
   (c) What is the motivation of an Array Processor [10+4+2]
5. (a) Explain the difference between Multiprocessor and Multi computer system.
   (b) What is computer module and explain non hierarchical loosely coupled multiprocessor system with neat diagram [4+12]
6. (a) Describe multicache problems? Describe methods to solve these problems.
   (b) Describe a methodology to evaluate different multiprocessor memory configurations. [8+8]
7. (a) Compare data driven and dependence driven computing models.
   (b) Explain the multilevel program abstraction in the event driven data flow computing model. [8+8]
8. (a) How memory mapping is done in Cyber-205? Explain
   (b) List various functions of virtual memory in Cyber 205.
   (c) Describe any two special vector instruction of Cyber 205. [8+4+4]

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Code No: RR410408 **Set No.3**

IV B.Tech. I Semester Regular Examinations, November -2005
ADVANCED COMPUTER ARCHITECTURE
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Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
All Questions carry equal marks

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1. (a) Describe at least four characteristics of MIMD microprocessors that distinguish them from multiple computer systems or.
   (b) Give Flynns classification of computer organizations and describe the salient features of each class. [8+8]
2. (a) What are precedence graph and reservation tables. What is their role in pipline systems?
   (b) Describe three different classes of data dependent hazards and illustrate the hazard conditions. [8+8]
3. (a) Explain the conceptual view of a single stage interconnection network and a switch.
   (b) Give basic organization of Illiac- IV array processor. Explain the its operation . [8+8]
4. (a) How is the Summation functionality performed in a SIMD Machine
   (b) Name some SIMD parallel algorithms and along with their complevity
   (c) What is the motivation of an Array Processor [10+4+2]
5. (a) With a block diagram explain the working of a single bus interconnection network for multiprocessor system. What are its advantages and drawbacks?
   (b) Explain briefly the following bus arbitration algorithms and give their relative merits.
      i. The static priority algorithm
      ii. The fixed time slice algorithm [10+6]
6. (a) Explian about static coherence check and dynamic coherence check.
   (b) Explain the functions of fork and join and cobegin and coend with relevant examples. [8+8]
7. (a) What is meant by data forwarding?
   (b) Explain the differences between sequential control flow and parallel control flow computer.
   (c) Explain how an instruction is executed in a control flow computer using shared data memory. [4+4+8]

8. (a) Explain about the performance evaluation of queuing models of a computer systems.
   (b) Explain about stochastic convergence of simulation models. [8+8]

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Code No: RR410408 **Set No.4**

IV B.Tech. I Semester Regular Examinations, November -2005
ADVANCED COMPUTER ARCHITECTURE
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Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
All Questions carry equal marks

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1. (a) What are interleaved memory organizations? What are the considerations in choosing these memory organizations for pipeline or vector processors?
   (b) Explain the S-access memory organization for pipeline vector processors with the help of neat diagrams depicting the configuration and the timing diagram of the configuration. [8+8]
2. Describe how Branch target buffering, and Register tagging improves the performance of pipelines. [8+8]
3. (a) Explain the connectivity of a barrel shifter for N = 8
   (b) List down the routing function for a plus-minus-2^i Network and compare with Illiac Network [10+6]
4. (a) Compare the two types of Associative Processor organizations
   (b) Differentiate between Bit-slice and Word-slice operations in STARAN [10+6]
5. (a) Explain briefly the communication between processors in a Multiprocessor environment.
   (b) With suitable diagram, explain loosely coupled and tightly coupled Multiprocessors. [6+10]
6. (a) When processes are said to be concurrent? Explain briefly Conway's fork-join concept.
   (b) Explain briefly reusable, consumable and virtual resources. [10+6]
7. (a) Explain a square systolic array for L-U decomposition.
   (b) Describe a matrix Arithmetic architecture processor. [8+8]
8. (a) Discuss about a simple queuing structure with a single processor having inter arrival time and service times.
   (b) Discuss in detail the performance of M/M/n queuing structure. [8+8]

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