Code No: NR410506 **NR**

IV B.Tech I Semester Supplementary Examinations, November 2005
FAULT TOLERANT SYSTEMS
(Common to Computer Science & Engineering and Electronics & Computer Engineering)

Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
All Questions carry equal marks

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1. Derive the reliability function of a parallel ,series system compare the results with a fixed R(t) = 0.9 for each module used. [6+6+4]
2. Write short notes on :
   (a) Random test vector generation
   (b) Transition count testing.
   (c) Compare the above 2 methods with conventional methods. [6+6+4]
3. (a) Explain the 5MR Reconfiguration scheme. Explain in detail the function of each block. [4+4]
   (b) Discuss the 3 cases for which the 5MR system automatically reconfigure to tolerate single and multiple faults. Explain each with an example. [3+3+2]
4. (a) With an example explain the practical fault tolerant system?
   (b) How do you enhance the fault tolerance characteristics of digital systems.[8+8]
5. Build a self-testing checker for any
   (a) systematic error detecting codes.
   (b) systematic error detecting codes like Berger codes with I =2^K - 1 data bits. [8+8]
6. (a) Explain the design consideration of self checking PLA considering stray faults with suitable example.
   (b) How do you implement strong fault service for the functional PLA. [8+8]
7. (a) What is meant by design for testability? What are the properties of a Design for testable circuit? Explain. [3+4+3]
   (b) How does controllability and observability take important role in design for testability? [3+3]
8. Explain observability enhancement with neat diagram with suitable examples. [4+2+10]

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