Code No: RR410505 **Set No. 1**

IV B.Tech I Semester Regular Examinations, November 2005
VLSI SYSTEMS DESIGN
(Common to Computer Science & Engineering, Computer Science & Systems Engineering and Electronics & Computer Engineering)

Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
All Questions carry equal marks

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1. Implement the following gates with CMOS Logic and explain its working
   (a) 2 Input NAND gate.
   (b) 3 Input NOR gate. [8+8]
2. (a) Define the terms SSI, MSI, LSI and VLSI.
   (b) Define the terms fan-out, fan-in, Propagation delay and noise margin of a logic-family. [8+8]
3. Design a stick diagram for CMOS two-input NAND and NOR gates. [16]
4. Compute the high-to-low delay of a two-input static complementary NOR gate with minimum-sized transistor driving these loads.
   (a) An inverter with minimum-sized pull up and pull down.
   (b) An inverter whose pull up and pull down are both of size $W = 10\lambda$ $L = 10\lambda$. [8+8]
5. Explain with suitable example the details of single - Row layout design method. [16]
6. Draw the circuit diagram of Depletion-load NMOS SRAM cell and explain its working principle. [16]
7. Explain clearly the global routing phase of the floor planning of the chip with few examples by considering all constraints. [16]
8. Sketch the architecture of the kitchen timer chip and explain about its architecture design. [16]

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Code No: RR410505 **Set No. 2**

IV B.Tech I Semester Regular Examinations, November 2005
VLSI SYSTEMS DESIGN
(Common to Computer Science & Engineering, Computer Science & Systems Engineering and Electronics & Computer Engineering)

Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
All Questions carry equal marks

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1. Implement the following gates with CMOS Logic and explain its working
   (a) 2 Input OR gate.
   (b) 4 Input NAND gate. [8+8]
2. (a) Define the terms Analog systems & Digital system with Two Examples.
   (b) Define the terms logic family, Saturated logic and non-saturated logic [8+8]
3. Explain with neat sketches CMOS fabrication using P - well process. [16]
4. Design a layout for NMOS 3- input NOR gate. [16]
5. Explain with suitable example the details of single - Row layout design method. [16]
6. Discuss clearly about the following system Design principles.
   (a) Pipelining
   (b) Data-paths [8+8]
7. How would you translate a register - transfer structure into a legal two - phase latched sequential machine? [16]
8. With suitable example explain any one of the scheduling algorithm [16]

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Code No: RR410505 **Set No. 3**

IV B.Tech I Semester Regular Examinations, November 2005
VLSI SYSTEMS DESIGN
(Common to Computer Science & Engineering, Computer Science & Systems Engineering and Electronics & Computer Engineering)

Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
All Questions carry equal marks

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1. Implement the following gates with CMOS Logic and explain its working
   (a) 2 Input NAND gate.
   (b) 3 Input NOR gate. [8+8]
2. What are the key advantages of ICs? And explain how these advantages of ICs translate in to advantages at the system level. [16]
3. Explain with neat sketches CMOS fabrication using twin - tub process. [16]
4. Design a layout for CMOS 2-input AND gate. [16]
5. Explain the procedure to optimize power consumption of an isolated logic gate.[16]
6. Draw the basic structure of serial-Parallel multiplier and explain its working principle. [16]
7. Clearly discuss about power distribution and clock distribution routing procedure. [16]
8. Draw the state transition graph for the kitchen timer chip's controller. [16]

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Code No: RR410505 **Set No. 4**

IV B.Tech I Semester Regular Examinations, November 2005
VLSI SYSTEMS DESIGN
(Common to Computer Science & Engineering, Computer Science & Systems Engineering and Electronics & Computer Engineering)

Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
All Questions carry equal marks

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1. Implement the following gates with CMOS Logic and explain its working
   (a) 2 Input OR gate.
   (b) 4 Input NAND gate. [8+8]
2. (a) Define the terms Analog systems & Digital system with Two Examples.
   (b) Define the terms logic family, Saturated logic and non-saturated logic [8+8]
3. Explain about different spice - parameters of MOS transistor and their significance. [16]
4. (a) What do you mean by layout of a component?
   (b) Draw neat layout diagram for NMOS transistor [8+8]
5. Explain the delay calculation procedure for CMOS inverter. [16]
6. Draw the structure of an un-signed array Multiplier and explain its working. [16]
7. How would you translate a register - transfer structure into a legal two - phase latched sequential machine? [16]
8. Clearly explain about the generic integrated circuit design flow. [16]

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