Code No: NR411905 **NR**

IV B.Tech I Semester Supplementary Examinations, November 2005
VLSI TECHNOLOGY
(Electronics & Computer Engineering)

Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
All Questions carry equal marks

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1. (a) Explain why a thin oxide layer is required in MOS fabrication ? [8]
   (b) What is meant by twin tube process and explain where it is used? [8]
2. (a) Explain different types of scaling models. Write down scaling factors used for these models.
   (b) Bring out the effects of scaling on the following parameters in all three models:
      i. Gate capacitance.
      ii. Maximum operating frequency.
      iii. Power speed product. [6+10]
3. (a) What are the different types of programmable inter connection channels used for routing parts in FPGAs? Explain
   (b) Explain about anti fuses used in FPGAs [8+8]
4. (a) Discuss in detail semi-custom layout styles. [8]
   (b) Explain in detail about the configurable logic blocks. [8]
5. Briefly explain the following verification tools: [4x4=16]
   (a) timing verifiers
   (b) design rule checkers
   (c) layout extractions and
   (d) test vectors.
6. Discuss the following types of simulations. [4+3+3+3+3]
   (a) circuit level
   (b) logic level
   (c) switch level
   (d) mixed mode and
   (e) timing simulations
7. (a) What are the various requirements while in designing package?
   (b) What is the difference between through hole and surface mount packages.[8+8]

8. (a) Prove that the combination of BJT and MOS technology offers the best performance in Analog VLSI design.

   (b) Draw the block diagram of D/A converter suitable for VLSI Analog Circuits and explain. [8+8]

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