Code No: RR410506 **Set No. 1**

IV B.Tech I Semester Regular Examinations, November 2005
FAULT TOLERANT SYSTEMS
(Common to Computer Science & Engineering and Electronics & Computer Engineering)

Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
All Questions carry equal marks

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1. (a) Define the term Reliability of a system. Derive a relation for the R(t) in terms of constant failure rate λ. [3+5]
   (b) What is meant by Mean time between failures? How is it useful in system usage. Derive the expression of MTBF. [2+3+3]
2. Show that the 3 paths indicated in the circuit cannot be sensitized individually but can be sensitized simultaneously as show in figure1. [16]

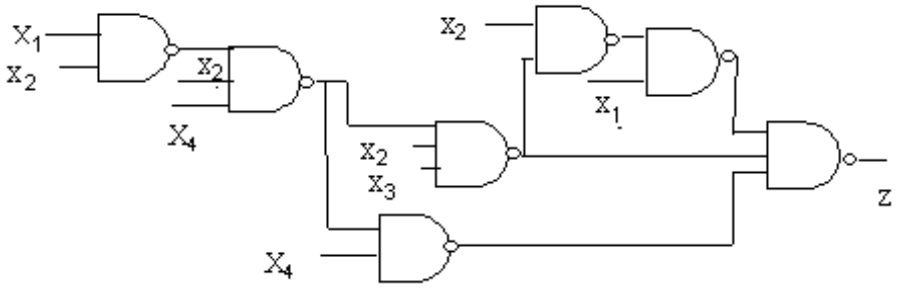

Figure 1:

3. (a) Explain the 5MR Reconfiguration scheme. Explain in detail the function of each block. [4+4]
   (b) Discuss the 3 cases for which the 5MR system automatically reconfigure to tolerate single and multiple faults. Explain each with an example. [3+3+2]
4. (a) What is the mechanism adopted in COPRA a fault Tolerant system. Explain in detail.
   (b) What is meant by Time redundancy? Explain. [4+4+4+4]
5. (a) Distinguish between Residue codes and Inverse Residue codes.
   (b) Explain in detail about checksum code.
   (c) With neat block diagram explain how the checking is done by residues.[6+5+5]
6. Design a sequential circuit using a partition theory for the given state table. [16]

PS	NS, I_1	I/P, I_2	Z I_3	I_4
A	C,0	C,0	A,0	A,0
B	B,1	C,0	D,1	A,0
C	C,0	B,0	A,0	A,0
D	B,1	A,0	D,1	A,0
E	E,0	E,0	A,0	A,0

7. (a) What is meant by design for testability? What are the properties of a Design for testable circuit? Explain. [3+4+3]

   (b) How does controllability and observability take important role in design for testability? [3+3]

8. (a) What is meant by circular BIST technique?

   (b) Give a simplified configuration of circular BIST and explain. [8+8]

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Code No: RR410506 **Set No. 2**

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FAULT TOLERANT SYSTEMS
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Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
All Questions carry equal marks

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1. (a) If a system has 4000 identical components with a failure rate of 0.02% per 1000 hours. Find the MTBF of such a system.
   (b) Explain the phenomenon of Bath tub response for a Time Vs failure rate of a system. [8+8]
2. (a) What is a tree live circuit. Give properties of tree like circuits.
   (b) For the given tree like circuit find the complete test set using path sensitizing method as show in figure1. [3+5+8]

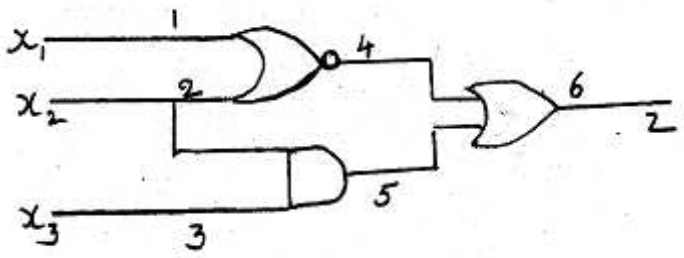

Figure 1:

3. (a) Explain the 5MR Reconfiguration scheme. Explain in detail the function of each block. [4+4]
   (b) Discuss the 3 cases for which the 5MR system automatically reconfigure to tolerate single and multiple faults. Explain each with an example. [3+3+2]
4. With an example explain :
   (a) software redundancy.
   (b) time redundancy. [8+8]
5. (a) What is the need for self checking circuits
   (b) Design a totally self checking checker by using reddy's partition method for 2out of 5 code. [6+10]
6. (a) Explain the general appraoch to the design of totally self-checking PLAs.
   (b) Explain why self-checking machines are essential in digital system. [10+6]

7. (a) Explain the Reed-Muller expansion Technique used in Design for testable circuit.

   (b) Obtain the Reed Muller circuit for the given function. Also give the test set for the same.
   $f = AB + \overline{AC} + BC$ [8+4+4]

8. (a) What is meant by built in test of VLSI? Explain.

   (b) Discuss the crosscheck approach to incorporate test circuitry into the basic cells used in implement VLSI design. [8+8]

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Code No: RR410506 **Set No. 3**

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Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
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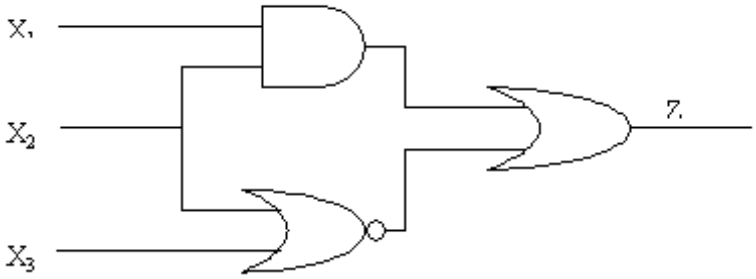
1. Derive the reliability function of a parallel ,series system compare the results with a fixed R(t) = 0.9 for each module used. [6+6+4]

2. (a) Illustrate the principles of path sensitizing method for the circuit given below and generate test vectors for different paths having different faults on them as shown in the figure1.



$Z = X_1X_2 + \overline{X}_2\overline{X}_3$

Figure 1:

   (b) How is path sensitization method advantageous over Fault Table method.Prove it for the above example. [8+8]

3. (a) With an example explain sift out modular redundancy technique.
   (b) With an example explain self-purging redundancy. [8+8]

4. (a) What is the mechanism adopted in COPRA a fault Tolerant system. Explain in detail.
   (b) What is meant by Time redundancy? Explain. [4+4+4+4]

5. (a) Design a combinational self - testing checkers for k - out of 2 k codes, which are self-testing.
   (b) List out the importance and advantages of self - checking checker circuits. [8+8]

6. Apply the procedure of designing a fail safe sequential machine using Berger code to the given state table. [16]

PS	NS, Z x=0	x=1
A	E,0	B,0
B	C,0	D,0
C	A,0	D,0
D	E,0	D,1
E	A,0	D,1

7. (a) What are the goals of a design for testability?
   (b) What are the different DET methods available? Explain at least two such techniques. [6+4+6]

8. (a) Discuss any one of the compression techniques that can be used in a BIST environment.
   (b) Write the principle behind the signature analysis technique. Explain with example. [8+8]

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Code No: RR410506 **Set No. 4**

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Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
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1. (a) If a system has 4000 identical components with a failure rate of 0.02% per 1000 hours. Find the MTBF of such a system.
   (b) Explain the phenomenon of Bath tub response for a Time Vs failure rate of a system. [8+8]

2. Using Boolean Difference Methods find the test vectors for SA0 fault on input line 1 and SA1 fault on the internal line 2 of the following circuit using all 6 methods as shown in figure1. [8+8]

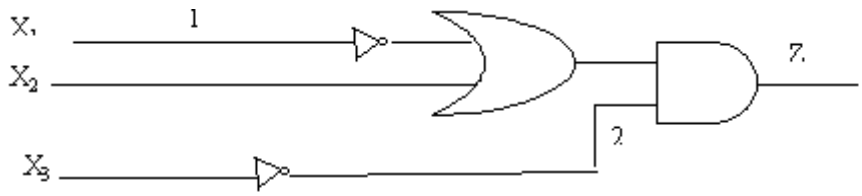

Figure 1:

3. (a) Explain the 5MR Reconfiguration scheme. Explain in detail the function of each block. [4+4]
   (b) Discuss the 3 cases for which the 5MR system automatically reconfigure to tolerate single and multiple faults. Explain each with an example. [3+3+2]

4. Explain the scheme proposed by lala for incorporating redundancy in the design of digital systems on single chip. [4+4+4+4]

5. (a) Construct a self-checking $\begin{bmatrix} 5 \\ 3 \end{bmatrix}$ code checker.
   (b) With neat block diagram explain in detail about self-checking realization of $\begin{bmatrix} n \\ k \end{bmatrix}$. [8+8]

6. Explain in detail about fail-safe sequential circuits design with an example. [16]

7. Write a short notes an [4x4=16]
   (a) Controllability

(b) Observability

(c) Positive unate function

(d) Syndrom relations of all types of terminating gates.

8. Explain observability enhancement with neat diagram with suitable examples. [4+2+10]

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