Code No: RR210202 **Set No. 1**

II B.Tech I Semester Supplementary Examinations, November 2006
PULSE AND DIGITAL CIRCUITS
(Common to Electrical & Electronic Engineering, Electronics & Communication Engineering, Electronics & Telematics and Electronics & Computer Engineering)

Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
All Questions carry equal marks

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1. (a) Verify $V_1 = \frac{V}{1+e^{-T/2RC}}$ $V_1' = \frac{V}{1+e^{T/2RC}}$ (figure1a)

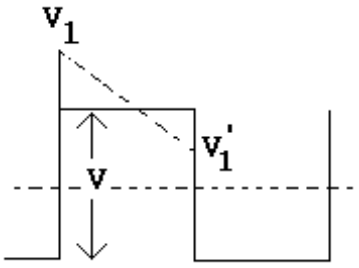

Figure 1a

For a symmetrical square wave applied to a high pass RC circuit. [10]

(b) Draw the RC high pass circuit and explain its working with step voltage input. [6]

2. (a) State and prove clamping-circuit theorem. [6]

(b) A square wave input as shown in figure 2b below is applied to the clamping circuit. Sketch the steady-state output waveform and derive the necessary expressions. [10]

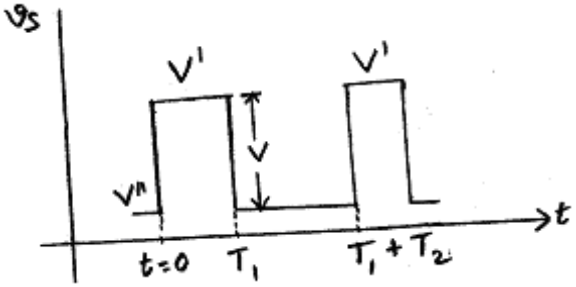

Figure 2b

3. (a) Explain in detail the junction diode switching times. [8]

(b) Give a brief note on piece-wise linear diode characteristics. [8]

4. (a) Discuss the symmetrical and Asymmetrical triggering in case of Bistable transistor multivibrator. [8]

(b) For the given circuit ,find UTP & LTP. What is this circuit called? Data given h_{fe}(min)=40, V_{CE}(sat)=0.1 V, U_{BE}(sat)=0.7 V V_r=0.5V, V_{BE}(active)=0.6V. (Figure 4b) [8]

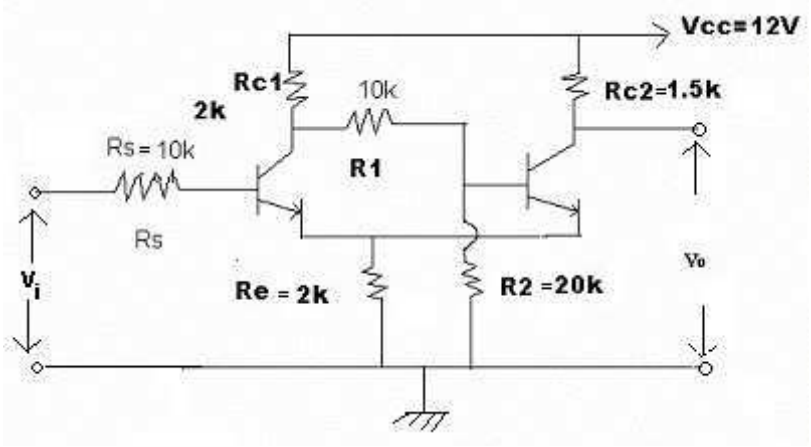

Figure 4b

5. (a) Define the three errors that occur in a sweep circuit and obtain an expression for these errors for an exponential sweep circuit. [8]

   (b) Explain with a circuit the working of a UJT sweep circuit and obtain the expressions for the intrinsic stand off ratio (η). [8]

6. (a) How astable multivibrator can be synchronized? Illustrate with waveforms.[8]

   (b) A symmetrical astable multivibrator using transistor operates from 10V supply has a period of 1msec. Triggering pulses of spacing 750 microsec are applied to one base through a small capacitor from a high-impedance source. Find the minimum triggering pulse amplitude required to achieve 1:1 synchronization. [8]

7. (a) Illustrate with neat circuit diagram, the operation of unidirectional sampling gate for multiple inputs. [8]

   (b) Explain with circuit diagram the operation of a two input sampling gate which does not have any loading effect on control signal. [8]

8. Consider the triggered blocking oscillator circuit shown in figure 8 below., using a silicon transistor with V_{CE} (sat) = 0.3V and V_{BE} (sat) = 0.7V and h_{FE} = 50. There are twice as many turns in the base winding as in the collector winding. The magnetizing inductance of the collector winding 3 mH , its leakage inductance is 50 μH and its shunt capacitance is 100 pF. During the pulse, calculate

   (a) the pulse amplitude at the collector [4]

   (b) the collector current [4]

   (c) the base current and [4]

   (d) the pulse width. [4]

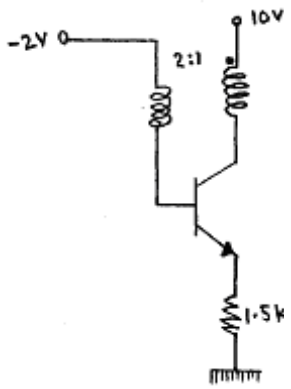

Figure 8

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Code No: RR210202 **Set No. 2**

II B.Tech I Semester Supplementary Examinations, November 2006
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Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
All Questions carry equal marks

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1. (a) Verify $V_1 = \frac{V}{1+e^{-T/2RC}}$ $V_1' = \frac{V}{1+e^{T/2RC}}$ (figure1a)

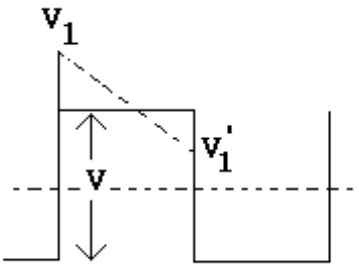

Figure 1a

For a symmetrical square wave applied to a high pass RC circuit. [10]

(b) Draw the RC high pass circuit and explain its working with step voltage input. [6]

2. (a) State and prove clamping-circuit theorem. [6]

(b) A square wave input as shown in figure 2b below is applied to the clamping circuit. Sketch the steady-state output waveform and derive the necessary expressions. [10]

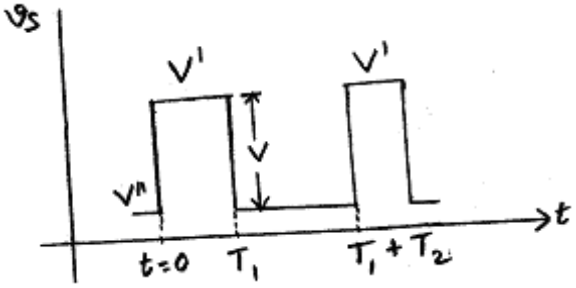

Figure 2b

3. (a) Explain how transistor can be used as a switch in the circuit, under what condition a transistor is said to be 'OFF' and 'ON' respectively. [6]

(b) A germanium transistor is operated at room temperature in the CE configuration. The supply voltage is 6 V, the collector-circuit resistance is 200 Ω and the base current is 20 percent higher than the minimum value required to drive the transistor into saturation. Assume the following transistor parameters: I_{co}=-5μA, I_{EO}=-2μA, h_{FE}=100, and $r_{bb'}$=250 Ω. Find V_{BE}(Sat) and V_{CE}(Sat). [10]

4. A transistor Schmitt trigger uses n-p-n silicion transistors with h_{fe}(min)=30 Vce(sat)=0.1v,V_{BE}(sat)=0.7v

   V_{cc}=12v,R_{c1}=2k R_{c2}=1kΩ, R_1=20kΩ, R_2=100kΩ, R_e=500Ω,Rs=2kΩ. (figure 4)

   (a) Draw the circuit diagram. Calculate all the steady-state currents & voltages. [8]

   (b) Determine UTP & LTP. [4]

   (c) Find Hystersis voltage. [2]

   (d) Sketch the output waveform if a triangular waveform as shown is applied to the circuit. [2]

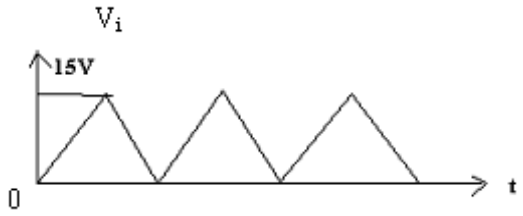

Figure 4

5. (a) Write important applications of time-base circuits. With reference to time base circuits define the following terms: [8]

      i. Flyback time

      ii. Transmission error.

   (b) What is meant by triggered sweep? What are the merits and demerits of triggered sweep circuits. [8]

6. (a) Bring out the importance of synchronization and frequency division. [8]

   (b) The relaxation oscillator when running freely, generates an output sweep amplitude of 100V and frequency 1kHz. Synchronizing pulses are applied such that at each pulse the breakdown voltage is lowered by 20V. Over what frequency range may the synchronizing pulse frequency be varied if 1:1 synchronization is to result? [8]

7. (a) What is a sampling gate? Explain the operation of series gate using JFET. Sketch the input and output waveforms. [8]

   (b) Illustrate the errors encountered in series sampling and what is the design procedure to minimize these errors? [8]

8. (a) Discuss the methods of controlling output current pulse width in blocking oscillators. [6]

   (b) Write notes on hysteresis effect in blocking oscillators. [4]

   (c) Discuss the method of improving rise time in blocking oscillator. [6]

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Code No: RR210202 **Set No. 3**

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Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
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1. (a) A symmetrical square wave of peak to peak amplitude V and frequency 'f ' is applied to a high pass RC circuit. Find the percentage tilt. [12]
   (b) How can this tilt be reduced? [4]

2. (a) Design a clipping circuit with ideal components, which can give the waveform shown in figure 2a below for a sinusoidal input. [8]

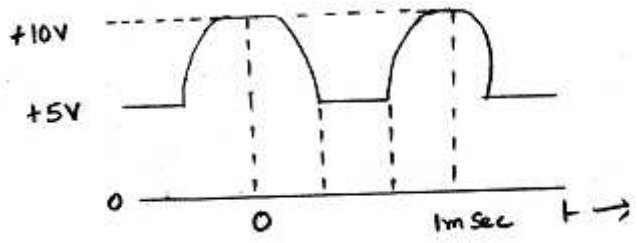

Figure 2a

   (b) Design a diode clamper to restore a d.c level of +3 Volts to an input signal of peak to peak value of 10 Volts. Assume drop across diode is 0.6 Volts. as shown in the figure (figure 2b)below [8]

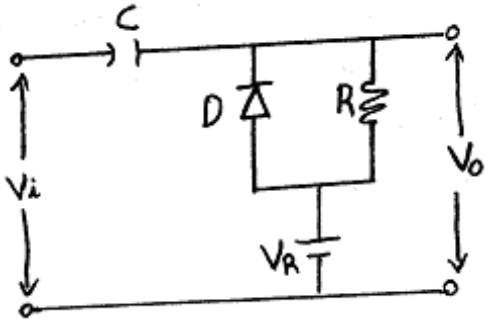

Figure 2b

3. (a) Explain the phenomenon of "latching" in a transistor switch. [6]
   (b) A transistor has f_T = 50 MHz, h_{FE}=40, $C_{b'c}$=3PF and operates with V_{cc}=12 V and R_c=500 Ω. The transistor is operating initially in the neighbourhood of the cut-in point. What base current must be applied to drive the transistor to saturation in 1μ sec? [10]

4. (a) Design a collector coupled astable multivibrator to meet the following specifications:

f=10KHZ,V_{CC}=12V,I_C (sat)=4mA and h_{FE}(min)=20.Assume that V_{CE} (sat)=0.3V and V_{BE} (sat)=0.7V. [8]

(b) An astable multi is used as a voltage to frequency converter. Find the ratio of V_{CC}/V,if the voltage to frequency converter generates oscillations of frequency thrice that when V=V_{CC}. [8]

5. (a) Distinguish between voltage and current time base generators. [6]

   (b) In the current-sweep circuit, how linearity can be corrected through adjustment of driving waveform. Illustrate with an example. [10]

6. (a) Explain how a sinusoidal oscillator can be used as a frequency divider. [8]

   (b) Write short notes on

      i. Phase delay and

      ii. Phase jitters [8]

7. (a) Distinguish between logic gate and sampling gate. [4]

   (b) Why is a sampling referred as a linear gate? [4]

   (c) Illustrate the principle of operation of a linear gate using series switch and shunts witch. What are the disadvantages? [8]

8. What is meant by blocking oscillator? Explain the principle of operation of monostable blocking oscillator with base timing. Sketch the current waveforms and derive an expression for current pulse width. [16]

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Code No: RR210202 **Set No. 4**

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Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
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1. (a) A pulse is applied to a low-pass RC circuit. Prove by direct integration that the area under the pulse is same as the area under the output waveform across the capacitor. Explain the result. [10]
   (b) Write a short notes on Highpass RC circuit as a differentiator. [6]
2. (a) What is synchronized clamping? Explain. [8]
   (b) Design a diode clamper circuit to clamp the positive peaks of the input signal at zero level. The frequency of the input signal is 500 Hz. [8]
3. (a) Describe the switching times of BJT by considering the charge distribution across the base region. Explain this for cut off, active and saturation regions. [8]
   (b) Define the following terms:
      i. storage time
      ii. delay time
      iii. rise time
      iv. fall time. [8]
4. Design a Monostable circuit that produces a pulse width of 10 m sec. Assume h_{fe}=30, V_{CE}(sat)=0.3V, V_{BE}sat=0.7V I_c=5mA, V_{cc}=6V. V_{BB}=1.5V, Q_1 ON and Q_2 OFF. [16]
5. (a) Bring out the necessity and importance of Time base circuits. [6]
   (b) In the UJT sweep circuit, V_{BB} = 20V, V_{yy} = 50V, R=5k, C=0.01 micro F. UJT has η= 0.5. Calculate
      i. amplitude of sweep signal
      ii. Slope and displacement errors and
      iii. estimated recovery time. [10]
6. (a) Explain about synchronization of a sweep circuits with symmetrical signals. - [8]
   (b) A UJT sweep operates with a valley voltage of V_v=2V and a peak voltage V_p=12V. A sinusoidal synchronizing voltage of 2V peak is applied between bases. The stand-off ratio is η=0.5. If the natural frequency of sweep is 1kHz, over what range of synchronizing signal frequency will the sweep remain in 1:1 synchronization with the synchronizing signal? [8]

7. (a) What is a sampling gate? Explain the operation of series gate using JFET. Sketch the input and output waveforms. [8]

   (b) Illustrate the errors encountered in series sampling and what is the design procedure to minimize these errors? [8]

8. In the circuit (figure 8) shown below, D is a germanium diode with $V_\gamma << V_{CC}$.

   (a) Explain why this circuit operates as high duty-cycle astable blocking oscillator [8]

   (b) Indicate the relative winding polarities [2]

   (c) Show that an approximately symmetrical square wave is obtained if $n_1 = n+1$ - [6]

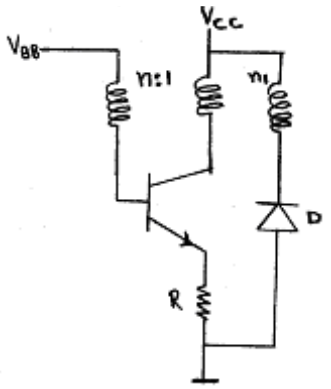

Figure 8

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