Code No: R059210505 **Set No. 1**

II B.Tech I Semester Regular Examinations, November 2006
COMPUTER ORGANIZATION
(Common to Computer Science & Engineering, Information Technology and Computer Science & Systems Engineering)

Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
All Questions carry equal marks

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1. (a) What are the different interconnection structures used in multiprocessors. Explain about multistage crossbar switch. [8]
   (b) Support or oppose the statement ?Every efficient serial program is efficient parallel program? [8]
2. Design register selection circuit to select one of the four 4-bit registers content on to bus. Give fuller explanation. [16]
3. (a) What are the major design considerations in microinstruction sequencing?. [8]
   (b) Explain about microinstruction sequencing techniques, specifically variable format address microinstruction. [8]
4. (a) Explain Booth's algorithm with its theoretical basis. [8]
   (b) Represent two n-bit unsigned numbers multiplications with a series of n/2-bit multiplications. [8]
5. (a) What is Redundant Array of Inexpensive Discs? What are the advantages of using this kind of systems?
   (b) Explain different levels of RAID [8+8]
6. Write short notes on the following:
   (a) DMA Controller
   (b) I O P
   (c) I/O Devices [6+6+4]
7. What is pipelining? Explain pipeline processing with an example. [16]
8. Write short notes on the following
   (a) Time-shared common bus organization [6]
   (b) Multiport memory organization [5]
   (c) System bus structure for multiprocessors [5]

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Code No: R059210505 **Set No. 2**

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Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
All Questions carry equal marks

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1. (a) Explain the terms compiler, linker, assembler, loader and describe how a C program or any other high level language program is executed in a system. Indicate entire process with a figure.
   (b) Distinguish between high level and low level languages?. What are the requirements for a good programming language? [16]
2. Design a circuit to increment, decrement, complement and clear a 4 bit register using RS flip-flops. Explain the control logic. [16]
3. (a) Give the typical horizontal and vertical microinstruction formats. [8]
   (b) Describe how microinstructions are arranged in control memory and how they are interpreted. [8]
4. (a) Multiply 10111 with 10011 using, Booths algorithm. [8]
   (b) Explain booths algorithm with its theoretical basis. [8]
5. Compare and contrast Asynchronous DRAM and Synchronous DRAM. [16]
6. (a) Explain bit oriented and character oriented protocols in serial communication
   (b) What are the different issues behind serial communication? Explain. [8+8]
7. (a) What is Flynn's classification? Categorize [6]
   (b) Explain each stream of the Flynn's classification with an example. [10]
8. (a) Explain the working of 8 x 8 Omega Switching network.
   (b) Explain the functioning of Binary Tree network with 2 x 2 Switches. Show a neat sketch [8+8]

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Code No: R059210505 **Set No. 3**

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Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
All Questions carry equal marks

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1. (a) Explain about sign magnitude and 2's complement approaches for representing the fixed point numbers. Why 2's complement is preferable.
   (b) Give means to identify whether or not an overflow has occurred in 2s complement addition or subtraction operations. Take one example for each possible situation and explain. Assume 4 bit registers.
   (c) Distinguish between tightly coupled microprocessors and tightly coupled Microprocessors. [16]
2. Mention about full adder circuit functionality with inputs and outputs using a block diagram. Using FA blocks design combined adder cum subtractor circuit. Assume two numbers are 4-bit numbers. [16]
3. (a) Why do we need subroutine register in a control unit?. Explain. [8]
   (b) Why do we need some bits of current microinstruction to generate address of the next microinstruction. Support with a live example. [8]
4. (a) Draw a flow chart which explains multiplication of two signed magnitude fixed point numbers. [8]
   (b) Multiply 10111 with 10011 with the above procedure given (a). Show all the registers content for each step. [8]
5. Compare and contrast Asynchronous DRAM and Synchronous DRAM. [16]
6. Explain the following:
   (a) Isolated Vs Memory mapped I/O
   (b) I/O Bus Vs Memory Bus
   (c) I/O Interface
   (d) Peripheral Devices [4+4+4+4]
7. Explain the following with related to the Instruction Pipeline
   (a) Pipeline conflicts
   (b) Data dependency
   (c) Hardware interlocks
   (d) Operand forwarding

(e) Delayed load

(f) Pre-fetch target instruction

(g) Branch target buffer

(h) Delayed branch [8×2=16]

8. (a) Explain the working of 8 x 8 Omega Switching network.

(b) Explain the functioning of Binary Tree network with 2 x 2 Switches. Show a neat sketch [8+8]

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Code No: R059210505 **Set No. 4**

II B.Tech I Semester Regular Examinations, November 2006
COMPUTER ORGANIZATION
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Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
All Questions carry equal marks

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1. (a) Explain about various buses such as internal, external, backplane, I/O, system, address, data, synchronous and asynchronous. [10]
   (b) Distinguish between high level and low level languages? What are the requirements for a good programming language? (6)
2. (a) Explain about stack organization used in processors. What do you understand by register stack and memory stack? [10]
   (b) Explain how X=(A+B)/(A-B) is evaluated in a stack based computer. [6]
3. Draw the general block diagram of a microsequencer. Explain clearly the inputs and outputs of the same along with their functioning. [16]
4. Draw a flowchart to explain how two IEEE 754 floating point numbers can be added, subtracted and multiplied. Assume single precision numbers. Give example for each [16]
5. (a) What is a virtual memory technique? Explain different virtual memory techniques. [8]
   (b) Explain how the technique of paging can be implemented [8]
6. (a) What is Direct Memory Access? Explain the working of DMA.
   (b) What are the different kinds of DMA transfers? Explain.
   (c) What are the advantages of using DMA transfers? [8+4+4]
7. (a) What is meant by arithmetic pipeline? Explain. [8]
   (b) Explain pipeline for floating point addition and subtraction. [8]
8. (a) Explain the working of 8 x 8 Omega Switching network.
   (b) Explain the functioning of Binary Tree network with 2 x 2 Switches. Show a neat sketch [8+8]

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