Code No: R059210404 **Set No. 1**

II B.Tech I Semester Regular Examinations, November 2006
ELECTRONIC CIRCUIT ANALYSIS
(Common to Electronics & Communication Engineering and Electronics & Telematics)

Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
All Questions carry equal marks

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1. (a) For a single stage transistor amplifier, R_S=200Ω and R_L= 5K . The h-parameter values are h_{fb}= - 0.98, h_{ib} =21 Ω, h_{rb} = 2.9 x10-4, h_{ob} = 0.49 μA/V. Find $A_I, A_V, A_{VS}, R_i, and R_o$ for the CB transistor configuration..
   (b) For a single stage transistor amplifier, RS=1KΩ and R_L= 10K The h-parameter values are h_{fe} = 50, h_{ie} =1.1KΩ, h_{re} = 2.5x10-4, h_{oe} = 25 μA/V. Find $A_I, A_V, A_{VS}, R_i, and R_o$ for the CE transistor configuration. (8+8)

2. (a) Draw the circuit of two stage R-C coupled JFET amplifier and explain its working.
   (b) Draw the circuit diagram of single stage R-C coupled BJTamplifier. Discuss the effect of an emitter bypass capacitor on low-frequency response. [8+8]

3. (a) Draw Hybrid - model for a transistor in the CE configuration and explain the significance of every component in this model.
   (b) Given a germanium p-n-p transistor whose basewidth is 10-4 cm. At room temperature and for a dc emitter current of 2 mA, find
      i. emitter diffusion capacitance,
      ii. fT [Assume Diffusion constant as 47 cm^2/sec] [8+8]

4. (a) Write short notes on requirement and types of heat sinks for power dissipation in large signal amplifiers.
   (b) With the help of a neat circuit diagram, explain the operation of a complementary symmetry configured class B power amplifier.
   (c) Compare and contrast push-pull and complementary-symmetry configurations for class B power amplifiers. [6+6+4]

5. (a) Explain in detail the need for tapped inductors in Tuned amplifiers?
   (b) Explain about synchronous tuning of Tuned amplifiers? [8+8]

6. (a) What is synchronous tuning ? Derive an expression for bandwidth of an n-stage synchronously tuned amplifier?
   (b) Show that for an 'n' stage synchronously tuned amplifier, maximum bandwidth is obtained when the single stage gain is 4.34dB. [8+8]

7. (a) What type of protection circuits are required in power supplies?

(b) A 50V power supply has line regulation 0.2%V. How large would the 75V input voltage to the supply have to become for the output voltage to rise to 52V?

(c) Give the disadvantages of the series and shunt regulators. [4+6+6]

8. (a) Explain different types of protections required in IC Voltage Regulators.

(b) Draw the block diagram of SMPS and explain its working with the help of waveforms [8+8]

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Code No: R059210404 **Set No. 2**

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ELECTRONIC CIRCUIT ANALYSIS
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Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
All Questions carry equal marks

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1. (a) Draw the circuit diagram of Common Drain amplifier and derive an expression for its Voltage gain.
   (b) The h-parameters of the transistor used in CE amplifier are h_{fe} = 50, h_{ie} =1.1KΩ, h_{re} = 2.5x10-4, h_{oe} = 24μ A/V. Find out current gain and voltage gains with and without source resistance , input and output impedances , given that R_L= 10K and R_S= 1 K. (6+10)

2. (a) Draw the circuit of two stage R-C coupled JFET amplifier and explain its working.
   (b) Draw the circuit diagram of single stage R-C coupled BJTamplifier. Discuss the effect of an emitter bypass capacitor on low-frequency response. [8+8]

3. (a) Draw the Hybrid - model of a transistor in CE configuration and give the typical values of these parameters.
   (b) Draw the small-signal equivalent circuit for an emitter- follower stage at high frequencies. Find its value of input admittance. [16]

4. (a) What is Harmonic distortion in transistor amplifier circuits? Discuss second harmonic distortion. [8]
   (b) A single transistor is operating as an ideal class B amplifier with a 500Ω load. A dc meter in the collector circuit reads 10mA. How much signal power is delivered to the load? [8]

5. (a) Draw the circuit diagram of a Double tuned amplifier. Draw and explain in detail the frequency response for different values of coefficient of coupling (K) i.e. K=1, K= 1.5, K=2 and also explain what is Loose coupling and Tight coupling?
   (b) Mention any four characteristics of double tuned amplifiers? [12+4]

6. Explain in detail the effect of cascading tuned amplifiers and hence derive the expression for bandwidth of n-stage amplifier. Also draw the frequency response and explain what happens as the number of stages increases? [16]

7. (a) Explain the terms
      i. Load Regulation
      ii. Line Regulation

iii. Stability factor

iv. Current limiting resistance

(b) Draw the functional block diagram of Series Voltage Regulator and explain each block. [8+8]

8. (a) What is catcher diode and explain the necessity of catches diode in Switch Regulator with the help of circuit diagram.

(b) List the operating ratings and electrical characteristics of IC 723. [8+8]

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Code No: R059210404 **Set No. 3**

II B.Tech I Semester Regular Examinations, November 2006
ELECTRONIC CIRCUIT ANALYSIS
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Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
All Questions carry equal marks

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1. (a) Discuss the classification of amplifiers based on frequency range , type of coupling ,power delivered , and signal handled.
   (b) For the Common Gate amplifier shown, derive expressions for voltage gain, input impedance and output impedance. Power supplies are omitted for simplicity. Neglect capacitances. [6+10]

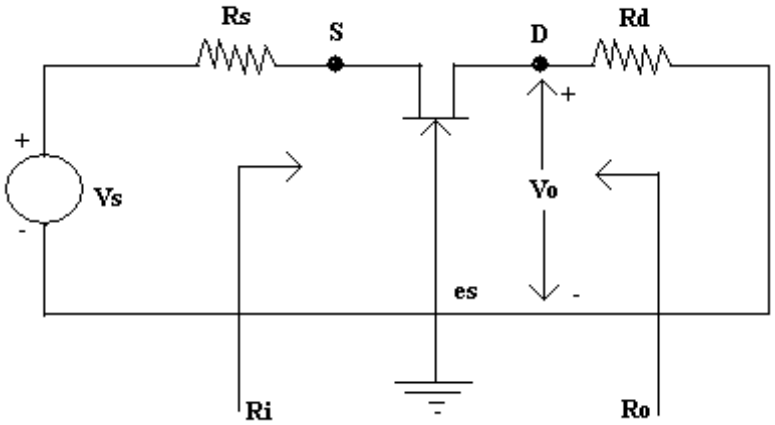

Figure 1

2. (a) Discuss about different types of distortions that occur in amplifier circuits
   (b) Three identical non interacting amplifier stages in cascade have an overall gain of 1 dB down at 30 Hz compared to mid band. Calculate the lower cutoff frequency of the individual stages. (8+8)

3. (a) In Hybrid - model of a transistor at high frequencies, show that is proportional to the collector current.
   (b) Define and what is physical significance of ? If a silicon p-n-p transistor has an What is the base thickness? [Assume Diffusion constant as 13 cm^2/sec] [16]

4. (a) Classify large signal amplifiers based on its operating point. Distinguish these amplifiers in terms of the conversion efficiency. [8]
   (b) Draw the push-pull power amplifier circuit. Derive the expression for the output current in push ?pull amplifier with base current as $i_b = I_{bm} \sin wt$. [8]

5. (a) Draw the circuit diagram and small signal AC equivalent circuit of a single tuned amplifier (using BJT) with the tank circuit connected at the input side.

(b) Draw the universal resonance curve for single tuned amplifier for different Values of 'Q' and explain?

(c) Also draw the phase response of a single tuned amplifier for increasing values of 'Q'? [8+4+4]

6. (a) Explain in detail about the Instability caused in tuned amplifiers at high frequencies?

(b) What is the importance of Stagger tuning? Explain briefly about Stagger tuned amplifiers? [8+8]

7. (a) The voltage regulator in Fig 7amaintains an output voltage of 25 V.

i. What value of Rsc should be used to limit the maximum current to 0.5A?

ii. With the value of Rsc found in (i) what will be the output voltage when RL= 100 ohms? When RL =10 ohms?

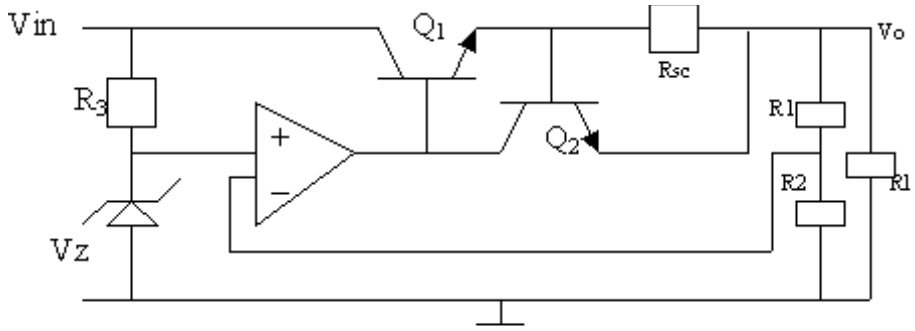

Figure 7a

(b) Draw and explain the regulator which will provide the foldback limiting .[8+8]

8. (a) Explain the significance of Low Pass Filter in Switching Regulator

(b) What are the limitations of Switching Regulators?

(c) Why switching frequencies are limited in Switching regulator and also explain how to overcome this. [6+4+6]

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Code No: R059210404 **Set No. 4**

II B.Tech I Semester Regular Examinations, November 2006
ELECTRONIC CIRCUIT ANALYSIS
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Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
All Questions carry equal marks

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1. (a) Using the h-parameter model, derive expressions for current gain, input impedance, voltage gain, and output impedance of a CE amplifier .
   (b) The h-parameters of a transistor are $h_{fe} = 50$, $h_{ie} = 1.1K\Omega$, $h_{re} = 2.5x10^{-4}$, $h_{oe} = 24\ \mu A/V$ Calculate A_I, A_V ,A_{VS} , R_i, and R_o. figure 1b

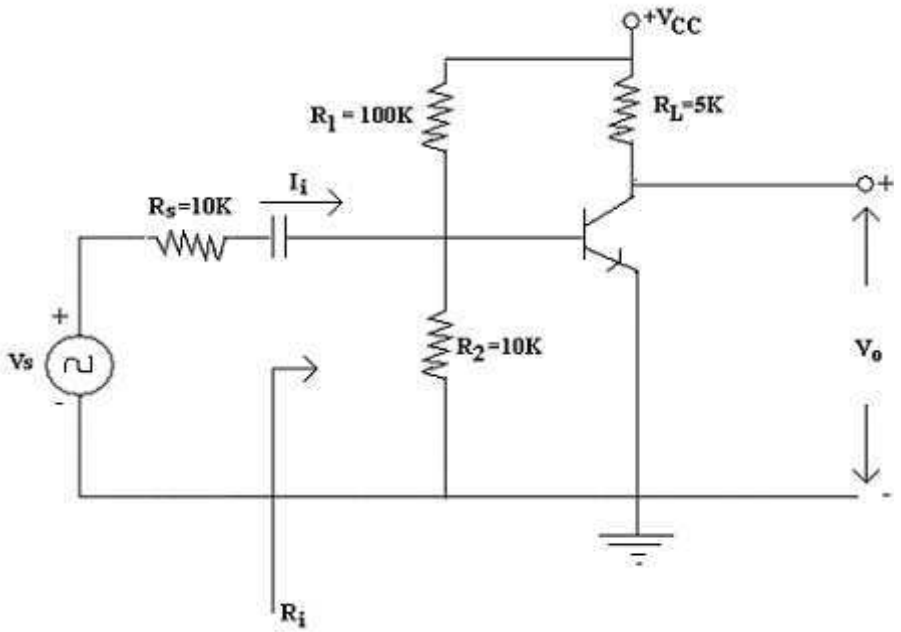

Figure 1b

2. (a) Derive the expression for the high 3-dB frequency f_H^* of n-identical non interacting stages in terms of f_H for one stage.
   (b) If four identical amplifiers are cascaded each having f_H =100 KHz, determine the overall upper 3dB frequency f^*H. Assume non interacting stages.
   (c) Write a short note on Bootstrapped Darlington circuit. (5+5+6)

3. (a) Derive the expression for the CE short circuit current gain A_i as a function of frequency using Hybrid - π model.
   (b) A single-stage CE amplifier is measured to have a voltage - gain bandwidth f_H of 5 MHz with $R_L = 500\Omega$. Assume $h_fe = 100$, g_m=100mA/V, $r_{bb'} = 100\Omega$, ,$C_c = 1pF$, and f_T =400MHz . Find the value of the source resistance that will give the required bandwidth.

4. (a) In transformer coupled Class ? A power amplifier, show that the conversion efficiency is 50%. [8]
   (b) Discuss in detail the cross-over distortion. How do you avoid the cross over distortion in power amplifier circuit? Discuss in detail. [8]

5. (a) Draw and explain the circuit diagram and equivalent circuit using high frequency hybrid - π model of a Single tuned Capacitance coupled BJT amplifier?
   (b) Also draw and explain the obtained modified high frequency equivalent circuit after applying Millers' theorem? [10+6]

6. Explain as to how you can increase the selectivity of single tuned amplifier. Draw the circuit diagram and explain its operation and also draw its frequency response? [16]

7. (a) The voltage regulator in Fig 7amaintains an output voltage of 25 V.
      i. What value of Rsc should be used to limit the maximum current to 0.5A?
      ii. With the value of Rsc found in (i) what will be the output voltage when RL= 100 ohms? When RL =10 ohms?

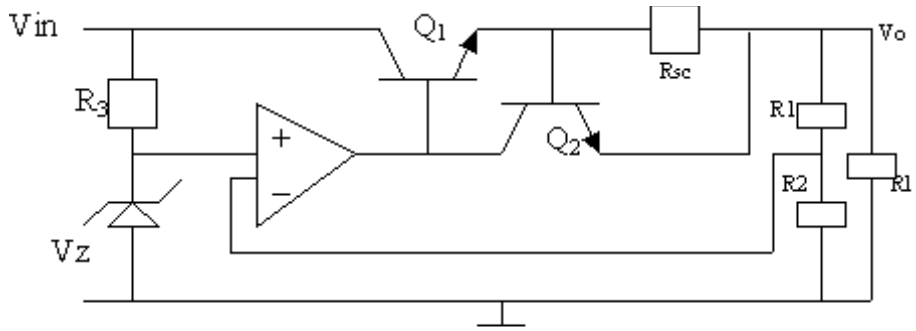

Figure 7a

   (b) Draw and explain the regulator which will provide the foldback limiting .[8+8]

8. (a) What is catcher diode and explain the necessity of catches diode in Switch Regulator with the help of circuit diagram.
   (b) List the operating ratings and electrical characteristics of IC 723. [8+8]

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