Code No: R059210504 **Set No. 1**

II B.Tech I Semester Regular Examinations, November 2006
DIGITAL LOGIC DESIGN
(Common to Computer Science & Engineering, Information Technology and Computer Science & Systems Engineering)

Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
All Questions carry equal marks

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1. (a) Express the Decimal Digits 0 - 9 in BCD, 2421, 84-2-1 and Excess-3.
   (b) Convert the Hexadecimal number 1010 to Decimal and then to Binary. [12+4]

2. (a) Express the following functions in sum of minterms and product of maxterms.
      i. F (A,B,C,D) = B'D + A'D + BD
      ii. F(x,y,z) = (xy + z)(xz + y).
   (b) Obtain the complement of the following Boolean expressions. [8+8]
      i. (AB' + AC')(BC + BC')(ABC)
      ii. AB'C + A'BC + ABC
      iii. (ABC)'(A + B + C)'
      iv. A + B'C (A + B + C').

3. (a) Implement the following Boolean function F using the two level forms NAND-AND, AND-NOR.
   $F(w, x, y, z) = \Sigma 0, 1, 2, 3, 4, 8, 9, 12$
   (b) Draw NOR-logic diagram that implements the following function: [8+8]
   $f(A, B, C, D) = \Sigma 0, 1, 2, 3, 4, 8, 9, 12.$

4. (a) Design a combinational logic circuit to compare two-two-bit binary numbers AB, CD in which A is MSB and D is LSB, to produce an output Z=1 whenever $AB \geq CD$ and Z = 0 if AB $<$ CD. Draw the circuit using NAND gates.
   (b) Draw the circuit diagram of a Full-subtractor using NOR gates. [8+8]

5. (a) Explain the following terms related to filp-flops.
      i. race round conditions
      ii. propagation delay
      iii. clock.
   (b) Explain the operation of R-S flip-flop with negative edge triggering with neat sketch. And explain its truth table. [8+8]

6. (a) Write the HDL structural description of the 4- bit universal shift register
   (b) Design a 4-bit ring counter using D- flip flops and draw the circuit diagram and timing diagrams. [8+8]

7. (a) Give the HDL code for a memory read , write operations if the memory size is 64 words of 4 bits each. Also explain the code

   (b) Obtain the 15-bit Hamming code for the 11-bit data word 11001001010. [8+8]

8. (a) What do you mean by hazard? Classify and explain.

   (b) Draw the logic diagram of the product of sums expression:
   Y= (x_1 + x_2') (x_2 + x_3). Show that there is a 0-hazard when x_1 and x_3 are equal to 0 and x_2 goes from 0 to 1. Find a way to remove the hazard by adding one or more OR gate. [8+8]

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1. (a) Perform the following using BCD arithmetic. Verify the result. [4+4]
   i. $7484_{10} + 3668_{10}$
   ii. $8254_{10} + 8277_{10}$
   (b) Convert the following:
   i. $A6_{16} = (\quad)_{10}$
   ii. $1266_8 = (\quad)_{10}$
   iii. $10100011_2 = (\quad)_{10}$
   iv. $372_{10} = (\quad)_{16}$ [2+2+2+2]

2. (a) Write short notes about the various digital logic families.
   (b) Obtain the complement of the following Boolean expressions.
   i. AB + A(B + C) + B'(B + D)
   ii. A + B + A'B'C.
   (c) Obtain the dual of the following Boolean expressions. [8+4+4]
   i. A'B + A'BC' + A'BCD + A'BC'D'E
   ii. ABEF + ABE'F' + A'B'EF.

3. (a) Implement the following Boolean expression with Excusive-NOR and NOR gates:
   $F = A\overline{B}C\overline{D} + \overline{A}BC\overline{D} + A\overline{B}\overline{C}D + \overline{A}B\overline{C}D$
   (b) If
   $F_1 = wx\overline{y} + \overline{y}z + \overline{w}y\overline{z} + \overline{x}y\overline{z}$ *And* $F_2 = (w + x + \overline{y} + \overline{z})(\overline{x} + \overline{y} + z)(\overline{w} + y + \overline{z})$
   Obtain minterms list of $F_1 \bullet F_2$ using K-map obtain minimal SOP function of $F_1 \bullet F_2$. [8+8]

4. (a) Generate 2's complement for the given 4 bit binary number using Full-adders. (Use only block diagram for Full adders)
   (b) Implement the following Boolean expressions with three half - adders.
   $D = A \oplus B \oplus C$
   $E = \overline{A}BC + A\overline{B}C$
   $F = AB\overline{C} + \left(\overline{A} + \overline{B}\right)C$
   $G = ABC$
   where A, B, C are the inputs and D, E, F, G are the outputs. [8+8]

5. (a) Define and explain the following systems.
   i. synchronous sequential systems,
   ii. a synchronous sequential systems and
   iii. combinational systems.
   (b) Define a latch. Explain the operation of NAND latch with truth table. [10+6]

6. (a) Explain synchronous and ripple counters. Compare their merits and demerits.
   (b) Design a modulo -12 up synchronous counter using T- flip flops and draw the circuit diagram. [8+8]

7. Derive the PLA programming table and the PLA structure for the combinational circuit that squares a 3- bit number. Minimize the number of product terms. [16]

8. (a) Explain critical and non critical races with the help of examples.
   (b) An asynchronous sequential circuit has two internal states and one output. The excitation and output functions describing the functions are: [6+10]

$$Y1 = x_1x_2 + x_1y_2' + x_2'y_1$$
$$Y2 = x_2 + x_1y_1'y_2 + x_1'y_1$$
$$Z = x_2 + y_1$$

   i. Draw the logic diagram of the circuit.
   ii. Derive the transition table and output map.
   iii. Obtain a flow table for the circuit.

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1. Convert the following to Decimal and then to Binary.
   (a) 1011_{16}
   (b) $ABCD_{16}$
   (c) 7234_8
   (d) 7766_8
   (e) 128_{10}
   (f) 720_{10} [3+3+3+3+2+2]

2. (a) Explain the concept of positive logic and negative logic. Also draw the truth tables for positive logic AND gate and negative logic OR gate.
   (b) Obtain the complement of the following Boolean expressions.
      i. B'C'D + (B + C + D)' + B'C'D'E
      ii. AB + (AC)' + (AB + C).
   (c) Obtain the dual of the following Boolean expressions. [8+4+4]
      i. A'B'C' + A'BC' + AB'C' + ABC'
      ii. AB + (AC)' + AB'C.

3. (a) Implement the following Boolean function F using no more than two NOR - gates and draw the circuit.
   $F(A, B, C, D) = \sum(0, 1, 2, 9, 11) + d(8, 10, 14, 15)$
   (b) Implement the following Boolean function using two - level forms: [6+10]
      i. NAND - AND
      ii. AND - NOR
      iii. OR - NAND and
      iv. NOR - OR and draw the circuits.
      $F(A, B, C, D) = \Pi 5, 7, 9, 11, 12, 13, 14, 15$

4. (a) Using 3 to 8 line de- multiplexers, construct 5 to 32 line de- multiplexers. Use active - low Enable input. If necessary use additional logic gates.
   (b) Design a combinational logic circuit with three inputs x, y, z and three outputs A, B, C. when the binary input is 0,1,2,or 3, the binary output is one greater than the input. When the binary input is 4,5,6,or 7 the binary output is one

less than the input. Draw the circuit using one- full adder and an inverter. (Use only block diagram of Full adder). [8+8]

5. A sequential circuit with 2 D-flip-flops A and B has two inputs (X, Y) and one output 'Z' with following relationship
D_A = (A+B)X, $D_B = \overline{A}$X, Z = (A+B)$\overline{X}$
Obtain logic diagram, state table and state diagram. [16]

6. A counter is to be designed to count either in 5421 code or 8421 code based on a control signal input. Draw the state diagram for such a counter and synthesize it using T flip flops. Assume that the control signal cannot change in the middle of a counting sequence. [16]

7. (a) What is parity checking? Explain its necessity and how is it implemented?
   (b) How many parity check bits must be included with the data word to achieve single error-connection and double-error detection when the data contains [8+8]
      i. 16 bits,
      ii. 32 bits,
      iii. 48 bits.

8. (a) Explain static and dynamic hazards in asynchronous sequential logic with an example.
   (b) Find a circuit that has no static hazards and implements the Boolean function. [8+8]

   F = Σ(0,2,6,7,8,10,12)

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1. Convert the following to Decimal and then to Hexadecimal.
   (a) 3214_8
   (b) 4567_8
   (c) 10101101_2
   (d) 1100101_2
   (e) 756_{10}
   (f) 533_{10} [3+3+3+3+2+2]

2. (a) Simplify the following Boolean expressions.
      i. A'C' + ABC + AC' to three literals
      ii. (x'y' + z)' + z + xy + wz to three literals
      iii. A'B(D' + C'D) + B(A +A'CD) to one literal
      iv. (A' + C)(A' + C')(A + B + C'D) to four literals.
   (b) Obtain the complement of the following Boolean expressions. [8+8]
      i. B'C'D + (B + C + D)' + B'C'D'E
      ii. AB + (AC)? + (AB + C)
      iii. A'B'C'+ A'BC' + AB'C' + ABC'
      iv. AB + (AC)' + AB'C.

3. (a) Obtain minimal SOP expression for the given Boolean function, using K-map: $F(A,B,C,D) = \Sigma(0,1,4,6,8,9,10,12) + d3,7,11,13,14,15$ And draw the circuit using 2-input NAND gates.
   (b) Obtain minimal POS expression for the Boolean function: $f(A,B,C,D) = \Pi(0,1,2,3,4,6,9,10) + d7,11,13,15$ And draw the circuit using 2-input NAND gates. [8+8]

4. (a) Generate 2's complement for the given 4 bit binary number using Full-adders. (Use only block diagram for Full adders)
   (b) Implement the following Boolean expressions with three half - adders.
   $D = A \oplus B \oplus C$
   $E = \overline{A}BC + A\overline{B}C$
   $F = AB\overline{C} + \left(\overline{A} + \overline{B}\right)C$
   $G = ABC$
   where A, B, C are the inputs and D, E, F, G are the outputs. [8+8]

5. (a) Draw the circuit diagram of clocked D- flip-flop with NAND gates and explain its operation using truth table. Give its timing diagram.
   (b) Explain the procedure for the design of sequential circuits with example. [8+8]
6. (a) Explain synchronous and ripple counters. Compare their merits and demerits.
   (b) Design a modulo -12 up synchronous counter using T- flip flops and draw the circuit diagram. [8+8]
7. (a) Explain the construction of a basic memory cell and also explain with diagram the construction of a 4 * 4 RAM
   (b) Given a 32*8 ROM chip with an enable input, show the external connections necessary to construct a 128 * 8 ROM with four chips and a decoder. [8+8]
8. (a) i. Explain the difference between asynchronous and synchronous sequential circuits.
      ii. Define fundamental-mode operation.
      iii. Explain the difference between stable and unstable states.
      iv. What is the difference between an internal state and a total state.
   (b) Explain critical and non critical races with the help of examples. [8+8]

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