Code No: RR210203 **Set No. 1**

II B.Tech I Semester Supplementary Examinations, November 2006
SWITCHING THEORY AND LOGIC DESIGN
(Common to Electrical & Electronic Engineering, Electronics & Communication Engineering, Computer Science & Engineering, Electronics & Instrumentation Engineering, Bio-Medical Engineering, Information Technology, Electronics & Control Engineering, Computer Science & Systems Engineering, Electronics & Telematics and Electronics & Computer Engineering)

Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
All Questions carry equal marks

⋆ ⋆ ⋆ ⋆ ⋆

1. (a) Write the following binary numbers in signed 1's complement form and signed 2's complement form using 16 bit registers.
   i. +1001010
   ii. -11110000
   iii. -11001100.1
   iv. +100000011.111
   (b) Perform N1+N2,N1+(-N2) for the following 8 bit numbers expressed in a 2's complement representation. Verify your answers by using decimal addition and subtraction
   i. N1=00110010, N2=11111101
   ii. N1=10001110, N2=00001101

   [10+6]

2. (a) i. Simplify the Boolean Expression X[Y+Z[$(\overline{XY + XZ})$] .
   ii. Obtain the simplified expression in SOP form of $\overline{x}\ \overline{z} + \overline{y}\ \overline{z} + y\overline{z} + xyz$.
   (b) Obtain the simplified expression in product of sums
   F(A, B, C,D) =$\sum$ (5, 6, 7, 8, 9, 12, 13, 14,).

   [4+4+8]

3. Use tabular procedure to simplify the given expression f(v,w,x,y,z) =$\sum$m(0,4,12,16,19,24,27,28,29,31) in SOP form and draw the circuit using only NAND gates. [16]

4. (a) Show how a 16-to-1 mux can be realized using 4-to-1 muxes.
   (b) Implement the function f(a,b,c)= a.b + $\bar{b}$.c using the 4-to-1 mux.

   [8+8]

5. (a) Define the following terms with related to Flip-Flop
   i. set-up time
   ii. hold-time

iii. propagation delay-time

(b) for the block diagram shown, draw the schematic circuit usinf NAND gates and explain its operation with help of truth-table. Shown in Figure 5 [6+10]

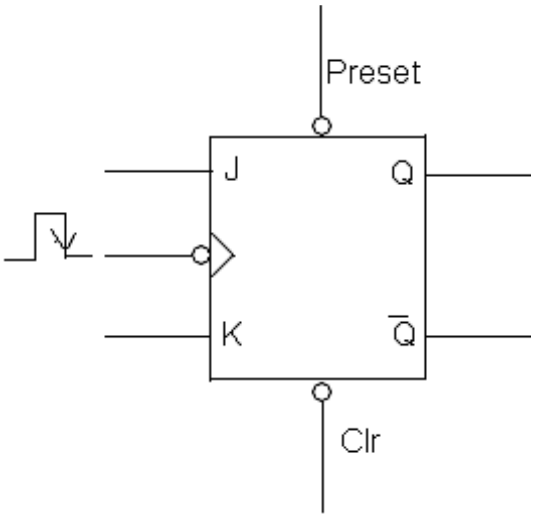

Figure 5

6. Design a 4-bit universal shift register and draw the circuit with the given mode of operation table.

S_1	S_0	Operation
0	0	Parallel
0	1	Shift right
1	0	Shift left
1	1	Inhibit clock

[16]

7. (a) Define state equivalance and machine equivalance with reference to sequential machines.

(b) Reduce the number of states in the following state table and tabulate the reduce state table and give proper assignment.

PS	NS,Z	
	X-0	X=1
A	F,0	B,0
B	D,0	C,0
C	F,0	E,0
D	G,1	A,0
E	D,0	C,0
F	F,1	B,1
G	G,0	H,0
H	G,1	A,0

[4+12]

8. (a) Draw the state diagram and the state table of the control unit for conditions given below. Draw the equivalent ASM chart leaving the state box empty.

i. from 00 state, if x = 1 , it goes to 01 state and if x = 0, it remains in the same state 00.
ii. from 01 state, if y = 1, it goes to 11 state and if y = 0, it goes to 10 state.
iii. from 10 stae, if x = 1 and y = 0, it remains in the same state 10 and if x = 1 and y = 1, it goes to 11 state, and if x = 0, it goes to 00 state.
iv. from 11 state, if x = 1, y = 0, it goes to 10 state and if x = 1, and y = 1, it remains in the same state, and if x = 0, it goes to 00 state.

(b) Design the control unit with multiplexers for the above problem

[8+8]

⋆ ⋆ ⋆ ⋆ ⋆

Code No: RR210203 **Set No. 2**

II B.Tech I Semester Supplementary Examinations, November 2006
SWITCHING THEORY AND LOGIC DESIGN
(Common to Electrical & Electronic Engineering, Electronics & Communication Engineering, Computer Science & Engineering, Electronics & Instrumentation Engineering, Bio-Medical Engineering, Information Technology, Electronics & Control Engineering, Computer Science & Systems Engineering, Electronics & Telematics and Electronics & Computer Engineering)

Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
All Questions carry equal marks

⋆ ⋆ ⋆ ⋆ ⋆

1. (a) Give the Gray-code equivalent of the Hex number 3A7.
   (b) Find the Gray-code equivalent of the octal number 527.
   (c) When a block of data is stored on magnetic tape, some times parity is computed on both the rows and columns. Create the row and column parity bits for the data group shown below using odd parity.
   DATA
   10110
   10001
   10101
   00010
   11000
   00000
   11010
   (d) Obtain the 3 bit and 4 bit Gray codes from the 2 bit Gray code by reflection.

   [4*4]

2. (a) i. Given $\overline{AB} + \overline{A}B = C$, Show that $\overline{AC} + \overline{A}C = B$.
      ii. $(A + B)(\overline{A} + C)(\overline{B} + D)(+C\overline{D})$;simplify
   (b) Define the connective * for the two valued variables A, B, and C as follows
   $A * B = AB + \overline{A}\ \overline{B}$
   Let C = A*B, Determine which of the following is valid
      i. A=B*C
      ii. B=A*C
      iii. A*B*C=1

   [8+8]

3. Implement the function F with the following two level forms
   (a) NAND-AND,
   (b) AND-NOR,

(c) OR-NAND and

(d) NOR-OR

$F(A, B, C, D) = \sum(0,1,2,3,4,8,9,12)$

[16]

4. (a) Design a combinational circuit that accepts a 3-bit number and generates an output binary number equal to the square of the input number.

   (b) Realize a 3-bit odd-parity generator circuit using only two-input ex-or gate

   [8+8]

5. (a) Define the following terms with related to Flip-Flop

   i. set-up time

   ii. hold-time

   iii. propagation delay ?time

   (b) For the block diagram(figure5b) shown, draw the schematic circuit using NAND gates and explain its operation with help of truth-table.

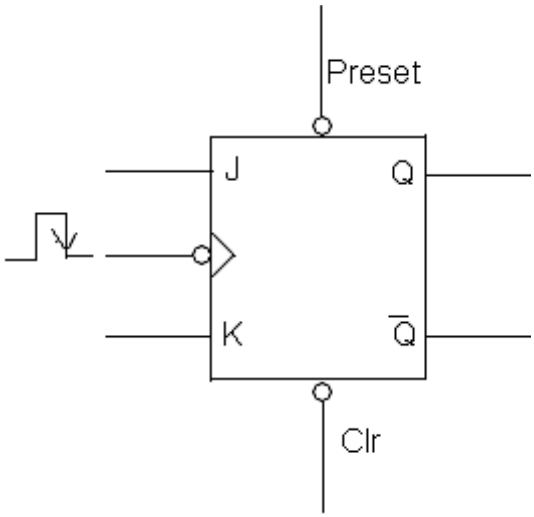

Figure 5b

6. Design a 4-bit universal shift register and draw the circuit with the given mode of operation table.

S_1	S_0	Operation
0	0	Parallel
0	1	Shift right
1	0	Shift left
1	1	Inhibit clock

[16]

7. What are the conditions for the two machines are to be equivalent? For the machine given below, find the equivalence partition and a corresponding reduced machine in standard form:

PS	NS,Z	
	X=0	X=1
A	F,0	B,1
B	G,0	A,1
C	B,0	C,1
D	C,0	B,1
E	D,0	A,1
F	E,1	F,1
G	E,1	G,1

[16]

8. (a) Draw the state diagram and the state table of the control unit for conditions given below. Draw the equivalent ASM chart leaving the state box empty.
   i. from 00 state, if x = 1 , it goes to 01 state and if x = 0, it remains in the same state 00.
   ii. from 01 state, if y = 1, it goes to 11 state and if y = 0, it goes to 10 state.
   iii. from 10 stae, if x = 1 and y = 0, it remains in the same state 10 and if x = 1 and y = 1, it goes to 11 state, and if x = 0, it goes to 00 state.
   iv. from 11 state, if x = 1, y = 0, it goes to 10 state and if x = 1, and y = 1, it remains in the same state, and if x = 0, it goes to 00 state.

   (b) Design the control unit with multiplexers for the above problem

[8+8]

⋆ ⋆ ⋆ ⋆ ⋆

Code No: RR210203 **Set No. 3**

II B.Tech I Semester Supplementary Examinations, November 2006
SWITCHING THEORY AND LOGIC DESIGN
(Common to Electrical & Electronic Engineering, Electronics & Communication Engineering, Computer Science & Engineering, Electronics & Instrumentation Engineering, Bio-Medical Engineering, Information Technology, Electronics & Control Engineering, Computer Science & Systems Engineering, Electronics & Telematics and Electronics & Computer Engineering)

Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
All Questions carry equal marks

⋆ ⋆ ⋆ ⋆ ⋆

1. (a) Devise a single error correcting code for a 11 bit group 01101110101
   (b) Test the following Hamming code sequence for 11 bit message and correct it if necessary (1010010111 01011).

   [8+8]

2. (a) Obtain the simplified expression in sum of products for the following Boolean functions using Karnaugh-Map.
      i. F(w,x,y,z) =$\sum$ (1,3,7,11,15) + $\sum_d$ (0, 2, 5)
      ii. F(A, B,C,D) = ABD+ $\overline{A}$ $\overline{C}$ $\overline{D}$+ $\overline{A}$ B+ $\overline{A}$ C $\overline{D}$+A $\overline{B}$ D
   (b) Show the truth table for each of the following function and find its simplest product of sums form.(POS)
      i. $f(x, y, z) = xy + xz$
      ii. $f(x, y, z) = \overline{x} + y\overline{z}$

   [8+8]

3. (a) Derive Boolean expression for a 2 input Ex-NOR gate to realize with two input NOR gates, without using complemented variables and draw the circuit.
   (b) Redraw the given circuit (figure3b) after simplification.

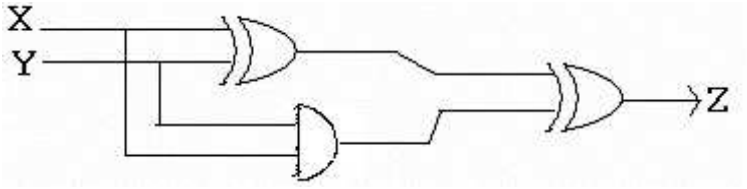

Figure 3b

   [8+8]

4. (a) Give the implementation of a 4-bit ripple-carry adder using half- adder(s) / full-adder(s).
   (b) Explain with an example , the mux and demux can be used as data - selector and data-distributor respectively.

   [8+8]

5. (a) Draw and explain with the help of truth table the logic diagram of a master slave D flip-flop using NAND gates. With active low preset and clear and with negative edge triggered clock.
   (b) Give the transition table for RS flip flop.
   (c) Convert JK flip flop into T and D flip flops.

[8+2+6]

6. Design a synchronous modulo 10 up down counter .Use T flip flops for synthesis. [16]

7. What are the conditions for the two machines are to be equivalent? For the machine given below, find the equivalence partition and a corresponding reduced machine in standard form:

PS	NS,Z	
	X=0	X=1
A	F,0	B,1
B	G,0	A,1
C	B,0	C,1
D	C,0	B,1
E	D,0	A,1
F	E,1	F,1
G	E,1	G,1

[16]

8. (a) Draw the state diagram and the state table of the control unit for conditions given below. Draw the equivalent ASM chart leaving the state box empty.
      i. from 00 state, if x = 1 , it goes to 01 state and if x = 0, it remains in the same state 00.
      ii. from 01 state, if y = 1, it goes to 11 state and if y = 0, it goes to 10 state.
      iii. from 10 stae, if x = 1 and y = 0, it remains in the same state 10 and if x = 1 and y = 1, it goes to 11 state, and if x = 0, it goes to 00 state.
      iv. from 11 state, if x = 1, y = 0, it goes to 10 state and if x = 1, and y = 1, it remains in the same state, and if x = 0, it goes to 00 state.
   (b) Design the control unit with multiplexers for the above problem

[8+8]

⋆ ⋆ ⋆ ⋆ ⋆

Code No: RR210203 **Set No. 4**

II B.Tech I Semester Supplementary Examinations, November 2006
SWITCHING THEORY AND LOGIC DESIGN
(Common to Electrical & Electronic Engineering, Electronics & Communication Engineering, Computer Science & Engineering, Electronics & Instrumentation Engineering, Bio-Medical Engineering, Information Technology, Electronics & Control Engineering, Computer Science & Systems Engineering, Electronics & Telematics and Electronics & Computer Engineering)

Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
All Questions carry equal marks

⋆ ⋆ ⋆ ⋆ ⋆

1. (a) Using 10's complement, subtract
   i. 72532-3250
   ii. 3250-72532. What do you infer from the results.
   (b) Decode the following ASCll code:
   1001010 1101111 1101000 1101110 0100000
   1000100 1101111 1100101
   Hint: Let us assume in decimal equivalent a=97, b=98, c=99.....z=122.

   [8+8]

2. (a) Obtain the simplified expression in sum of products for the following Boolean functions using Karnaugh-Map.
   i. F(w,x,y,z) =$\sum$ (1,3,7,11,15) + $\sum_d$ (0, 2, 5)
   ii. F(A, B,C,D) = ABD+ $\overline{A}$ $\overline{C}$ $\overline{D}$+ $\overline{A}$ B+ $\overline{A}$ C $\overline{D}$+A $\overline{B}$ D
   (b) Show the truth table for each of the following function and find its simplest product of sums form.(POS)
   i. $f(x, y, z) = xy + xz$
   ii. $f(x, y, z) = \overline{x} + y\overline{z}$

   [8+8]

3. Using the Quine-Mc Cluskey method of tabular reduction ,minimize the given combinational single - output function f(w,x,y,z) = $\sum$m(0,1,5,7,810,14,15) [16]

4. (a) Implement the following function with a mux F (a,b,c,d) = $\sum m(1, 3, 5, 6)$, choose a and b as select inputs.
   (b) Give the logic implementation of a 32 x 4 bit ROM using decoder of a suitable size.

   [8+8]

5. (a) With the help of block-diagrams, explain the difference between synchronous sequential circuit and Asynchronous sequential circuit and compare them.

(b) For the block diagram(figure5b) shown below, draw the schematic circuit using NAND gates and explain its working with the help of Truth-Table.

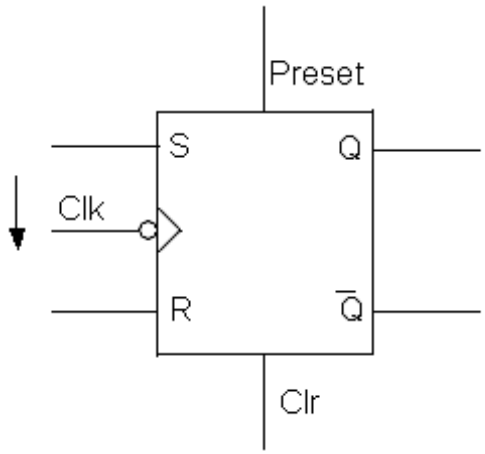

Figure 5b

[6+10]

6. Design a 4-bit universal shift register and draw the circuit with the given mode of operation table.

S_1	S_0	Operation
0	0	Parallel
0	1	Shift right
1	0	Shift left
1	1	Inhibit clock

[16]

7. (a) Explain the limitations of finite-state machines.

   (b) Find the equivalence partition and a corresponding reduced machine in standard form for the machine given below:

PS	NS,Z	
	X=0	X=1
A	E,0	D,1
B	F,0	D,0
C	E,0	B,1
D	F,0	B,0
E	C,0	F,1
F	B,0	C,0

[6+10]

8. (a) Design a digital system with three 4-bit registers, A, B and C to perform the following operations by drawing the ASM chart.

   i. Transfer two binary numbers to A and B when a start signal is enabled.

   ii. If A<B, shift left the contents of A and transfer the result to register C.

   iii. If A>B, shift right the contents of B and transfer the result to register C.

iv. If A+B, transfer the number to register C unchanged.

(b) Realize the above using JK flipflops and D flip flops.

[8+8]

⋆ ⋆ ⋆ ⋆ ⋆