Code No: R059210202 **Set No. 1**

II B.Tech I Semester Regular Examinations, November 2006
PULSE & DIGITAL CIRCUITS
(Common to Electrical & Electronic Engineering, Electronics & Communication Engineering, Electronics & Instrumentation Engineering and Electronics & Telematics)

Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
All Questions carry equal marks

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1. (a) Explain the response of a high pass circuit to an exponential input is applied.
   (b) Write short note on piping process. [8+8]

2. (a) Explain transfer characteristics of the emitter coupled clipper and derive the necessary equations.
   (b) Draw the basic circuit diagram of positive peak clamper circuit and explain its operation. [8+8]

3. Write Short notes on:
   (a) Diode switching times
   (b) Switching characteristics of transistors
   (c) FET as a switch. [4+8+4]

4. (a) Design a collector coupled transistor monostable multivibrator to produce a time delay of 100 μsec. Use transistors have h_{FE} of 250. Use $\pm$12v sources, $V_{CE(sat)} = 0.3$v, $V_{BE(sat)} = 0.7$v and $V_{BEcutoff} = 0$v
   (b) Show that the astable multivibrator works as voltage controlled oscillator. [10+6]

5. (a) Draw and explain the typical waveform of a time-base voltage.
   (b) Explain the principle of working of exponential sweep circuit with neat circuit diagram and also derive the equations for slope , transmission and displacement error. [6+10]

6. (a) Explain the factors which influence the stability of a relaxation divider with the help of a neat waveforms.
   (b) A UJT sweep operates with Vv = 3V, Vp=16V and η=0.5. A sinusoidal synchronizing voltage of 2V peak is applied between bases and the natural frequency of the sweep is 1kHz, over what range of sync signal frequency will the sweep remain in 1:1 synchronism with the sync signal? [8+8]

7. (a) What is sampling gate? Explain how it differ from Logic gates?
   (b) What is pedestal? How it effects the output of a sampling gates?
   (c) What are the drawbacks of two diode sampling gate? [6+6+4]

8. (a) What are the basic logic gates which perform almost all the operations in Digital communication systems.
   (b) Give some applications of logic gates.
   (c) Define a positive and negative logic systems.
   (d) Draw a pulse train representing a 11010111 in a synchronous positive logic digital system. [4+4+4+4]

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Code No: R059210202 **Set No. 2**

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Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
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1. (a) A square wave of 5 V amplitude with an ON time of 1 msec and an OFF time of 3 m sec is applied to a high pass RC circuit with R = 2K and C = 0.1 μ f. Sketch the steady state output waveform showing all the details
   (b) Explain the operation of RC high pass circuit when exponential input is applied. [8+8]
2. (a) Draw the circuit diagram of slicer circuit using Zener diodes and explain its operation with the help of its transfer characteristic.
   (b) Draw the circuit diagram of emitter coupled clipper. Draw its transfer characteristics indicating all intercepts, slopes and voltage levels derive the necessary equations. [8+8]
3. (a) Sketch neatly the waveforms of current & voltages for a transistor switch with capacitance loading circuit.
   (b) What are catching diodes? [12+4]
4. (a) Explain the reason for the occurrence of overshoot at the base of normally ON transistor of one shot. Derive an expression for overshoot.
   (b) Discuss a few applications of a monostable multivibrator. Explain how it differs with that of a binary. [8+8]
5. (a) How are linearly varying current waveforms generated?
   (b) In the boot strap circuit shown in figure5 V_{cc} = 25 V, V_{EE} = -15 V, R = 10 K ohms, R_B = 150 K ohms, C = 0.05 μF. The gating waveform has a duration of 300 μs. The transistor parameters are h_{ie} = 1.1Kohms, h_{re} = 2.5 x 10^{-4} K ohmsh_{fe} =50 h_{oe} = 1/40K ohms.
      i. Draw the waveform of IC1 and Vo , labeling all current and voltage levels,
      ii. What is the slope error of the sweep?
      iii. What is the sweep speed and the maximum value of the sweep voltage?
      iv. What is the retrace time Tr for C to discharge completely?
      v. Calculate the recovery time T1 for C1 to recharge completely. [6+10]

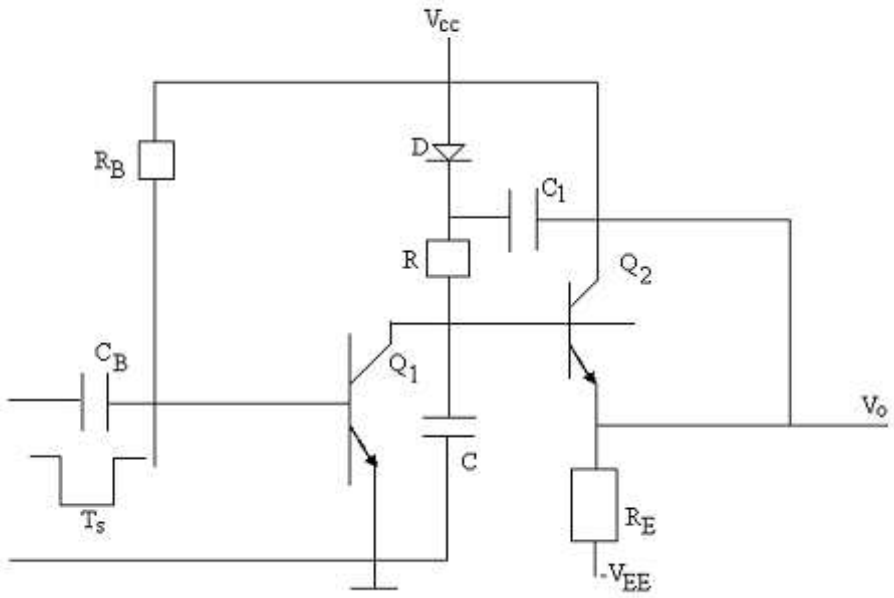

Figure 5

6. (a) What do you mean by synchronization ?
   (b) What is the condition to be met for pulse synchronization?
   (c) Compare sine wave synchronization with pulse synchronization? [4+6+6]

7. (a) Draw and explain an emitter coupled bi-directional sampling gate.
   (b) For the four diode gate shown in figure 7 with a divider resistance R used . V_s=25V, R_f=20 ohms, R_L=R_C=200K ohms and R= 100 ohms. Find V_{cmin}, A and V_{nmin}? [8+8]

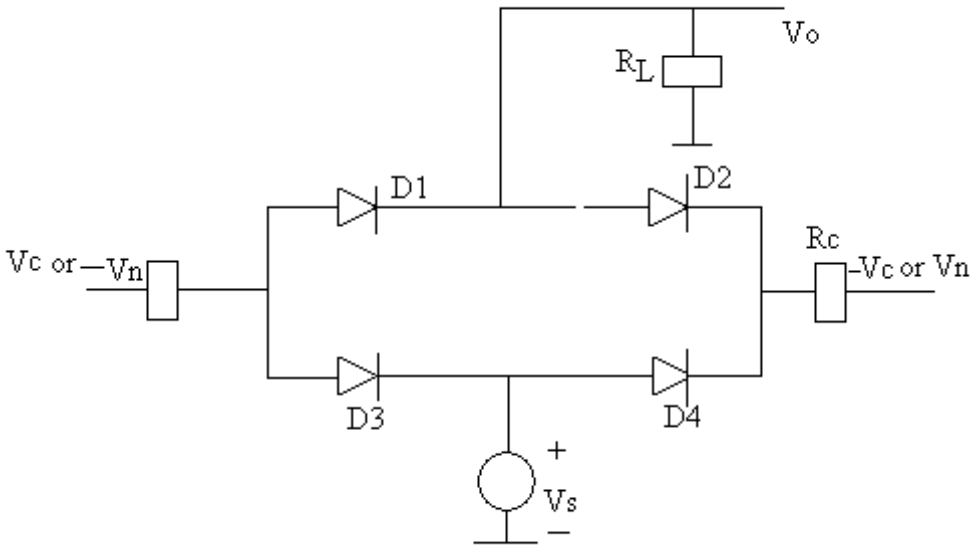

Figure 7

8. (a) What are the basic logic gates which perform almost all the operations in Digital communication systems.
   (b) Give some applications of logic gates.
   (c) Define a positive and negative logic systems.
   (d) Draw a pulse train representing a 11010111 in a synchronous positive logic digital system. [4+4+4+4]

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Code No: R059210202 **Set No. 3**

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Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
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1. (a) An ideal 1 μ -Sec pulse is fed to a low pass circuit. Calculate and plot the output waveform under the following conditions: The upper 3-dB frequency is
   i. 10 MHz
   ii. .1 MHz
   iii. .0.1 MHz.
   (b) Explain RLC ringing circuit. [10+6]

2. (a) Design a clipping circuit with ideal components, which can give the waveform shown in figure 2a for a sinusoidal input.

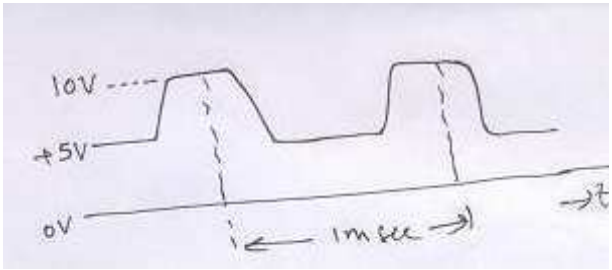

Figure 2a

   (b) State and prove clamping circuit theorem. [8+8]

3. (a) Sketch neatly the waveforms of current & voltages for a transistor switch with capacitance loading circuit.
   (b) What are catching diodes? [12+4]

4. (a) Explain the operation of Astable multivibrator with a circuit diagram with relevant waveforms.
   (b) A collector coupled monostable multi using n-p-n silicon transistor has the following parameters Vcc = 12v, V_{BB} = 3v, R_C = 2k, R1 = R2 = R = 20k, h_{FE} = 30, r_{bb} = 200 Ω and c = 1000pF. Calculate and plot to scale the wave slopes at each base and collector. Also find width of the o/p pulse. [8+8]

5. (a) What type of Voltage input is required to obtain a linear current sweep?
   (b) The transistor bootstrap circuit shown in Figure 5 has the following parameters V_{CC} = 10 V, V_{EE} = -10V, R_B = 30 K ohms, C=0.002 μF, C_1=0.25μF

and C_B may be taken as arbitrarily large. The input gate has an amplitude of 1V and a width of 50μs. The transistor parameters are $h_{FE} = h_{fe} = 60$, h_{ie}=2kohms, $1/h_{oe}$ = 10 K ohms, $h_{re} = 10^{-4}$. $I_{CBO} = 0$, and the forward biased junction voltages are negligible. The diode is ideal.

i. Plot the gate voltage, collector current i_{C1}, and the output voltage Vo.
ii. Evaluate the sweep speed and amplitude of the sweep at its maximum value
iii. Find time it takes to discharge C at the end of the sweep,
iv. Find peak voltage change across C_1 and the time required to replace the lost charge
v. Find slope error. [6+10]

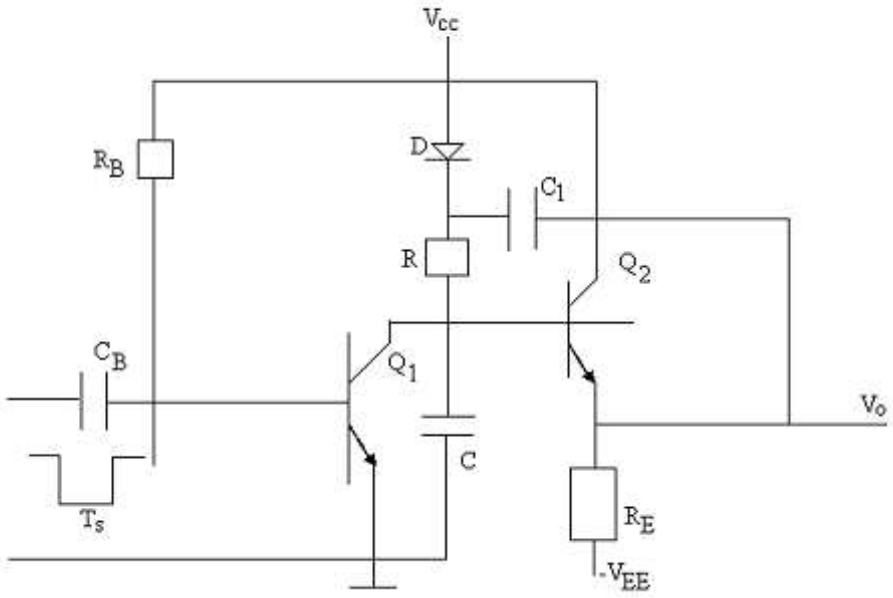

Figure 5

6. (a) What do you mean by synchronization ?
   (b) What is the condition to be met for pulse synchronization?
   (c) Compare sine wave synchronization with pulse synchronization? [4+6+6]

7. (a) With the help of a neat diagram, explain the working of two-diode sampling gate.
   (b) Derive expressions for gain and minimum control voltages of a bi-directional two- diode sampling gate. [8+8]

8. (a) Draw and explain the circuit diagram of a diode AND gate for positive logic.
   (b) Derive the output equation for a diode OR gate for positive logic. [8+8]

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Code No: R059210202 **Set No. 4**

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Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
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1. (a) Explain double differentiator with the help of neat sketches.
   (b) A limited ramp is applied to an RC differentiator. What is the peak of the out put wave form for
      i. T = RC
      ii. T= 0.2RC
      iii. T= 5RC. [8+8]

2. (a) State and prove clamping -circuit theorem.
   (b) A clamping circuit and input wave form is shown in figure 2b calculate and plot to scale the steady state output [8+8]

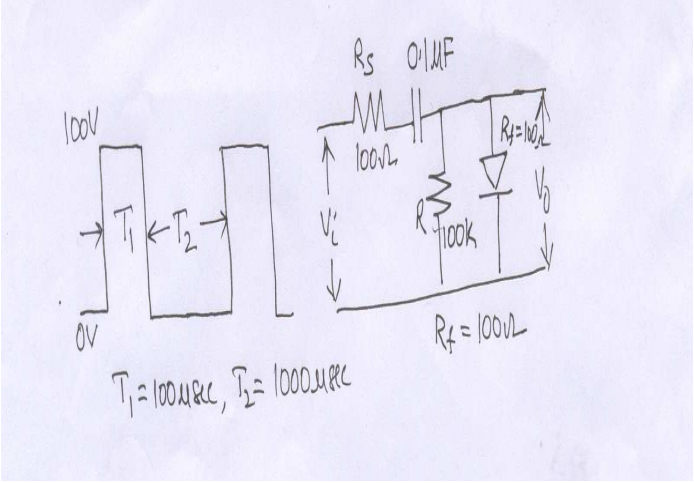

Figure 2b

3. (a) Describe the switching times of BJT by considering the charge distribution across the base region. Explain this for cut-off, active and saturation region.
   (b) Explain phenomenon of latching in a transistor. [12+4]

4. (a) Draw the circuit diagram of a Schmitt trigger circuit and explain its operation. Derive the Expressions for its UTP and LTP.
   (b) Explain how an Schmitt trigger circuit acts as a comparator. [12+4]

5. (a) What is a Linear time base generator? Give its Applications
   (b) Write the differences between the voltage and current time base generators?

(c) Why the time base generators are called sweep circuits? [6+6+4]

6. (a) What is relaxation oscillator? Name some negative resistance devices used as relaxation oscillators and give its applications.

   (b) With the help of a circuit diagram and waveforms, explain the frequency division by an astable multivibrator? [8+8]

7. (a) What is sampling gate? Explain how it differ from Logic gates?

   (b) What is pedestal? How it effects the output of a sampling gates?

   (c) What are the drawbacks of two diode sampling gate? [6+6+4]

8. (a) Why totem pole is used in DTL? Draw the circuit diagram and explain a DTL gate with this.

   (b) Verify the truth table of RTL NOR gate with the circuit diagram of two inputs. [8+8]

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