Code No: R059210203 **Set No. 1**

II B.Tech I Semester Regular Examinations, November 2006
SWITCHING THEORY & LOGIC DESIGN
(Common to Electrical & Electronic Engineering, Electronics & Instrumentation Engineering, Bio-Medical Engineering, Electronics & Control Engineering, Electronics & Computer Engineering and Instrumentation & Control Engineering)

Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
All Questions carry equal marks

⋆ ⋆ ⋆ ⋆ ⋆

1. (a) Generate Hamming code for the given 11 bit message 10001110101 and rewrite the entire message with Hamming code. [8]
   (b) The binary numbers listed have a sign bit in the left most position and, if negative numbers are in 2's complement form. Perform the arithmetic operations indicated and verify the answers. [4 × 2 = 8]
      i. 101011 + 111000
      ii. 001110 + 110010
      iii. 111001 - 001010
      iv. 101011 - 100110

2. (a) Reduce the following Boolean Expressions [8]
      i. AB + A(B + C) + B'(B + D)
      ii. A +B + A'B'C
      iii. A'B + A'BC' + A'BCD + A'BC'D'E
      iv. ABEF + AB(EF)' + (AB)'EF
   (b) Obtain the Dual of the following Boolean expressions. [8]
      i. x'yz + x'yz' + xy'z' + xy'z
      ii. x'yz + xy'z' + xyz + xyz'
      iii. x'z + x'y + xy'z + yz
      iv. x'y'z' + x'yz' + xy'z' + xy'z + xyz'

3. (a) Simplify the Boolean expression using K-map F= $(ABC\bar{D}) + (A) + (AB\bar{D}) + (\bar{D})(\bar{A}\bar{B}\bar{C})$. [8]
   (b) Reduce the following function using K- map and identify the prime implicant and non prime implicant .F= $\sum m(2, 3, 6, 7, 10, 11, 12)$. [8]

4. (a) Design a Excess-3 adder using 4-bit parallel binary adder and logic gates.
   (b) Draw the logic diagram of a single bit comparator. [12+6]

5. (a) Derive the PLA programming table for the combinational circuit that squares a 3 bit number.

(b) For the given 3-input, 4-output truth table of a combinations circuit,tabulate the PAL programming table for the circuit. [8+8]

Inputs			Output			
x	y	z	A	B	C	D
0	0	0	0	1	0	0
0	0	1	1	1	1	1
0	1	0	1	0	1	1
0	1	1	0	1	0	1
1	0	0	1	0	1	0
1	0	1	0	0	0	1
1	1	0	1	1	1	0
1	1	1	0	1	1	1

6. (a) Find a modulo-6 gray code using k-Map & design the corresponding counter.
   (b) Compare synchronous & Asynchronous. [8+8]

7. A clocked sequential circuit is provided with a single input x and single output Z. Whenever the input produce a string of pulses 1 1 1 or 0 0 0 and at the end of the sequence it produce an output Z = 1 and overlapping is also allowed.
   (a) Obtain State - Diagram.
   (b) Also obtain state - Table.
   (c) Find equivalence classes using partition method & design the circuit using D - flip-flops. [4+4+8]

8. (a) Draw the ASM chart for the following state transistion, start from the initial state T_1, then if xy=00 go to T_2, if xy=01 go to T_3, if xy=10 go to T_1, other wise go to T_3.
   (b) Show the exit paths in an ASM block for all binary combinations of control variables x, y and z, starting from an initial state. [8+8]

⋆ ⋆ ⋆ ⋆ ⋆

Code No: R059210203 **Set No. 2**

II B.Tech I Semester Regular Examinations, November 2006
SWITCHING THEORY & LOGIC DESIGN
(Common to Electrical & Electronic Engineering, Electronics & Instrumentation Engineering, Bio-Medical Engineering, Electronics & Control Engineering, Electronics & Computer Engineering and Instrumentation & Control Engineering)

Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
All Questions carry equal marks

⋆ ⋆ ⋆ ⋆ ⋆

1. (a) Perform the following using BCD arithmetic. [2 × 4 = 8]
   i. $7129_{10} + 7711_{10}$
   ii. $8124_{10} + 8127_{10}$
   (b) Convert the following. [4 × 2 = 8]
   i. $AB_{16} = (\quad)_{10}$
   ii. $1234_8 = (\quad)_{10}$
   iii. $10110011_2 = (\quad)_{10}$
   iv. $772_{10} = (\quad)_{16}$

2. (a) Simplify the following Boolean expressions to minimum no. of literals. [8]
   i. x'y' + xy + x'y
   ii. xy' + y'z' + x'z'
   iii. x'? + xy + xz' + xy'z'
   iv. (x + y)(x + y')
   (b) Obtain the complement of the following Boolean expressions. [8]
   i. AB + A(B + C) + B‘(B + D)
   ii. A + B + A‘B'C
   iii. A'B + A‘BC' + A'BCD + A‘BC‘D'E
   iv. ABEF + ABE‘F' + A‘B'EF

3. Apply Branching method to simplify the following function
   F (A, B, C, D) = $\prod M(0, 1, 4, 5, 9, 11, 13, 15, 16, 17, 25, 27, 28, 29, 31)d(20, 21, 22, 30)$. [16]

4. (a) Design a Excess-3 adder using 4-bit parallel binary adder and logic gates.
   (b) Draw the logic diagram of a single bit comparator. [12+6]

5. (a) Find the function f(x_1, x_2, x_3, x_4) realized by each of the threshold networks shown in the figure 5(a)i, 5(a)ii, 5b. [8+8]

i.

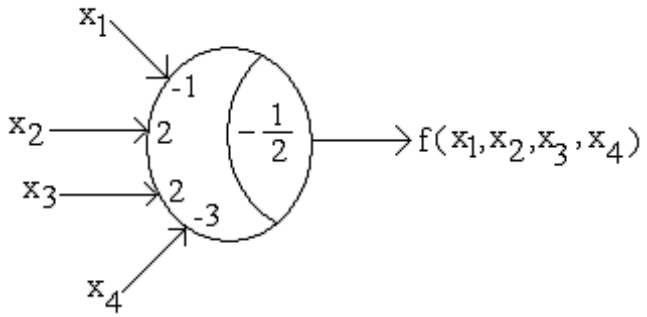

Figure 5(a)i

ii.

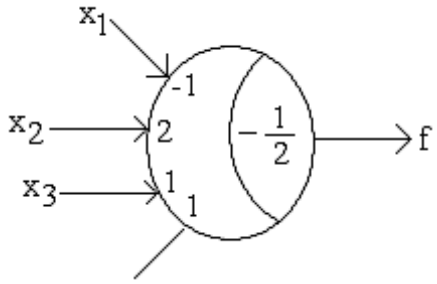

Figure 5(a)ii

(b)

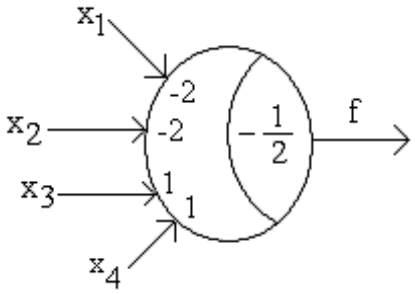

Figure 5b

6. (a) Give the design of 4 bit Ring counter and explain a with the waveforms. Also give the application of this ring counter.
   (b) Design a modulo-9 counter T flipflops with preset and clear inputs. [8+8]

7. A clocked sequential circuit is provided with a single input x and single output Z. Whenever the input produce a string of pulses 1 1 1 or 0 0 0 and at the end of the sequence it produce an output Z = 1 and overlapping is also allowed.
   (a) Obtain State - Diagram.
   (b) Also obtain state - Table.
   (c) Find equivalence classes using partition method & design the circuit using D - flip-flops. [4+4+8]

8. For the ASM chart given 8:

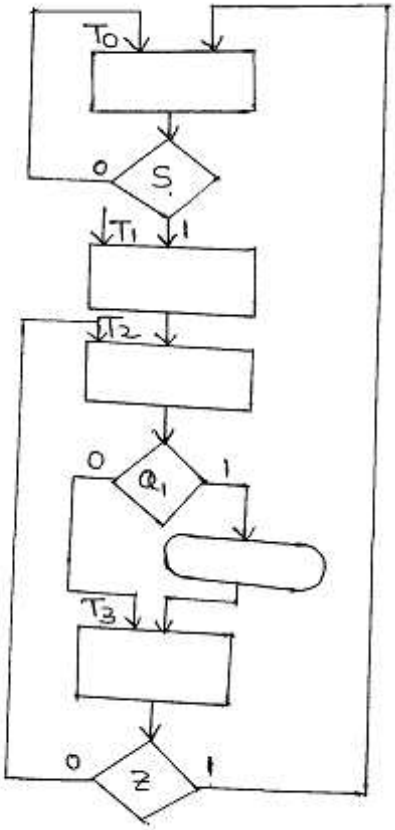

Figure 8

(a) Draw the state diagram.

(b) Design the control unit using D flip-flops and a decoder. [8+8]

⋆ ⋆ ⋆ ⋆ ⋆

Code No: R059210203 **Set No. 3**

II B.Tech I Semester Regular Examinations, November 2006
SWITCHING THEORY & LOGIC DESIGN
(Common to Electrical & Electronic Engineering, Electronics & Instrumentation Engineering, Bio-Medical Engineering, Electronics & Control Engineering, Electronics & Computer Engineering and Instrumentation & Control Engineering)

Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
All Questions carry equal marks

⋆ ⋆ ⋆ ⋆ ⋆

1. Convert the following to Decimal and then to Octal.
   (a) 4234_{16}
   (b) $125F_{16}$
   (c) 10010011_2
   (d) 10111111_2
   (e) 392_{10}
   (f) 779_{10} [3+3+3+3+2+2]

2. (a) Simplify the following expressions and implement them with NAND gate circuits. [8]
      i. AB' + ABD + ABD' + A'C'D' + A'BC'
      ii. BD + BCD' + AB'C'D'
   (b) Obtain the Dual of the following Boolean expressions.
      i. AB + A(B + C) + B'(B + D)
      ii. A + B + A'B'C [4]
   (c) Obtain the complement of the following Boolean expressions.
      i. A'B + A'BC' + A'BCD + A'BC'D'E
      ii. ABEF + ABE'F' + A'B'EF [4]

3. Minimise on the map the five variable function.
   F= $\sum m(0, 1, 4, 5, 6, 13, 14, 15, 22, 24, 25, 28, 29, 30, 31)$. [16]

4. (a) Design a 32:1 Multiplexer using two 16:1 and 2:1Multiplexers.
   (b) Design a circuit to convert Excess-3 code to BCD code Using a 4-bit Full adder. [8+8]

5. (a) Given a 32 x 8 Rom clip with an enable input, show the external connection necessary to construct a 128 x 8 Rom with four chips and a decoder.

(b) Tabulate the PLA programming table for the four Boolean functions listed below
A(x,y,z) = ε(1, 2, 4, 6)
B(x,y,z) = ε(0, 1, 6, 7)
C(x,y,z) = ε(2,6)
D(x,y,z) = ε(1, 2, 3, 5, 7). [8+8]

6. (a) Compare synchronous & Asynchronous circuits
   (b) Design a Mod-6 synchronous counter using J-K flip flops. [6+10]

7. A clocked sequential circuit is provided with a single input x and single output Z. Whenever the input produce a string of pulses 1 1 1 or 0 0 0 and at the end of the sequence it produce an output Z = 1 and overlapping is also allowed.
   (a) Obtain State - Diagram.
   (b) Also obtain state - Table.
   (c) Find equivalence classes using partition method & design the circuit using D - flip-flops. [4+4+8]

8. (a) Draw the ASM chart for the following state transistion, start from the initial state T_1, then if xy=00 go to T_2, if xy=01 go to T_3, if xy=10 go to T_1, other wise go to T_3.
   (b) Show the exit paths in an ASM block for all binary combinations of control variables x, y and z, starting from an initial state. [8+8]

⋆ ⋆ ⋆ ⋆ ⋆

Code No: R059210203 **Set No. 4**

II B.Tech I Semester Regular Examinations, November 2006
SWITCHING THEORY & LOGIC DESIGN
(Common to Electrical & Electronic Engineering, Electronics & Instrumentation Engineering, Bio-Medical Engineering, Electronics & Control Engineering, Electronics & Computer Engineering and Instrumentation & Control Engineering)

Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
All Questions carry equal marks

⋆ ⋆ ⋆ ⋆ ⋆

1. (a) Generate Hamming code for the given 11 bit message 10010110101 and rewrite the entire message with Hamming code. [8]
   (b) The binary numbers listed have a sign bit in the left most position and,if negative numbers are in 2's complement form. Perform the arithmetic operations indicated and verify the answers. [4×2=8]
      i. 101011 + 111001
      ii. 001111 + 110010
      iii. 111001 - 011010
      iv. 101111 - 100110

2. (a) Draw the logic diagram using only two input NAND gates to implement the following expression. [8]
   (AB + A'B')(CD'? + C'D)
   (b) Obtain the complement of the following Boolean expressions.
      i. B'C'D + (B + C + D)' + B'C'D'E
      ii. AB + (AC)' + (AB + C) [4]
   (c) Obtain the dual of the following Boolean expressions.
      i. A'B'C' + A'BC' + AB'C' + ABC'
      ii. AB + (AC)' + AB'C [4]

3. (a) Differentiate prime implicant and non prime implicant, essential prime implicant and non essential prime implicant. [8]
   (b) Reduce the following function using K- map and identify prime implicants and essential prime implicants F= $\sum m(0, 1, 2, 3, 6, 7, 13, 15)$ [8]

4. (a) Design a 32:1 Multiplexer using two 16:1 and 2:1Multiplexers.
   (b) Design a circuit to convert Excess-3 code to BCD code Using a 4-bit Full adder. [8+8]

5. Write a brief note on:
   (a) Architecture of PLDS
   (b) Capabilities and the limitations of thusold gates. [8+8]

6. (a) Compare synchronous & Asynchronous circuits
   (b) Design a Mod-6 synchronous counter using J-K flip flops. [6+10]

7. A clocked sequential circuit with simple input x and single output Z produce an output Z = 1 whenever the input x completes the sequence 1 0 1 1 and overlapping is allowed.
   (a) Obtain its state - diagram.
   (b) Obtain its minimal state - table and design the circuit with D - Flip-Flops. [8+8]

8. (a) For the given state-diagram of a control circuit 8 obtain ASM chart.
   (b) Design the circuit using multiplexers. [8+8]

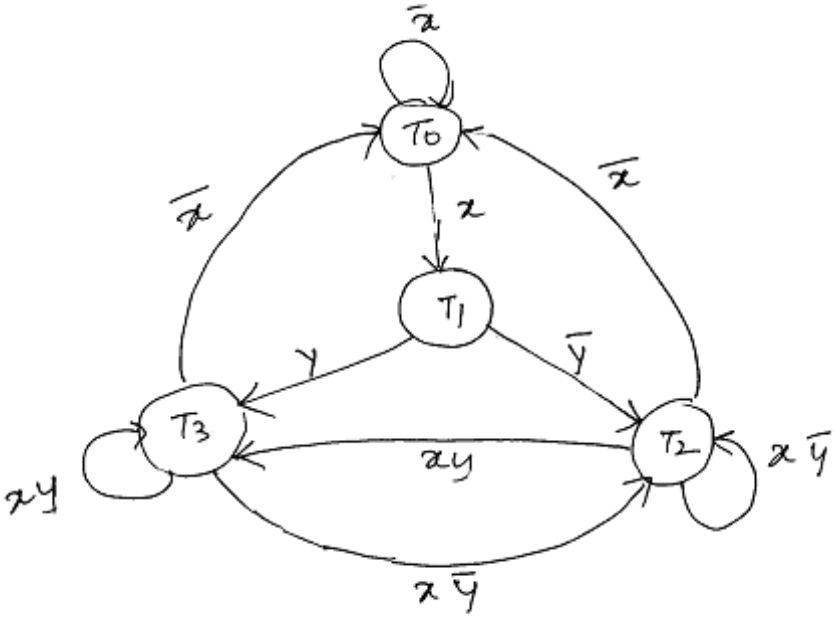

Figure 8

⋆ ⋆ ⋆ ⋆ ⋆