Code No: NR210203 **NR**

II B.Tech I Semester Supplementary Examinations, November 2006
SWITCHING THEORY & LOGIC DESIGN
(Common to Electrical & Electronic Engineering, Electronics & Communication Engineering, Computer Science & Engineering, Electronics & Instrumentation Engineering, Information Technology, Electronics & Control Engineering, Computer Science & Systems Engineering, Electronics & Telematics and Electronics & Computer Engineering)

Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
All Questions carry equal marks

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1. (a) Write the following binary numbers in signed 1's complement form and signed 2's complement form using 16 bit registers.
   i. +1001010
   ii. -11110000
   iii. -11001100.1
   iv. +100000011.111
   (b) Perform N1+N2,N1+(-N2) for the following 8 bit numbers expressed in a 2's complement representation. Verify your answers by using decimal addition and subtraction
   i. N1=00110010, N2=11111101
   ii. N1=10001110, N2=00001101

[10+6]

2. (a) Simplify the function using Karnaugh map method
   F (A,B,C,D) = $\sum$(4,5,7,12,14,15)+ $\sum$d(3,8,10).
   (b) Give three possible ways to express the function
   F = $\overline{A}\ \overline{B}\ \overline{D} + \overline{A}\ \overline{B}\ \overline{C}\ \overline{D} + \overline{A}BD + AB\overline{C}D$ with eight or less literals. [8+8]

3. (a) Derive Boolean expression for a 2 input Ex-NOR gate to realize with two input NOR gates, without using complemented variables and draw the circuit.
   (b) Redraw the given circuit (figure3b) after simplification.

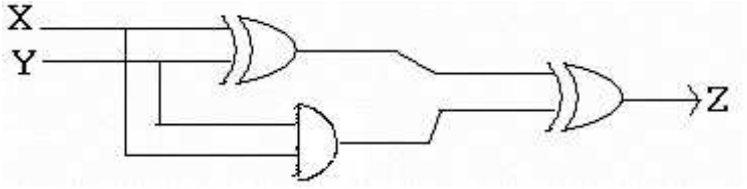

Figure 3b

[8+8]

4. Design a PLA to realize the following three logic functions and show the internal connections

$F_1(a,b,c,d,e) = \overline{a}\overline{b}\ \overline{d} + \overline{b}c\overline{d} + \overline{a}bcd\overline{e}$
$F_2(a,b,c,d,e) = \overline{a}be + \overline{b}c\overline{d}e$
$F_3(a,b,c,d,e) = \overline{a}\overline{b}\ \overline{d} + \overline{b}c\overline{d}e + \overline{a}bcd$ [16]

5. (a) Define a combinational system and a sequential system and how does they differ from each other

   (b) Draw the schematic circuit of "Master-slave J-K-Flip-Flop" using NAND gates and explain its operation with the help of Truth-Table.

   [8+8]

6. Design a sequential circuit with two D- flipflops A and B and one input x. When x=0, the state of the circuit remains the same. When x=1, the circuit goes through the state transitions from 00 to 01 to 11 to 10 back to 00 and repeats. [16]

7. Find the equivalence partition for the given machine. Show a standard form of the corresponding reduced machine.

PS	NS,Z	
	X=0	X=1
A	F,0	B,1
B	G,0	A,1
C	B,0	C,1
D	C,0	B,1
E	D,0	A,1
F	E,1	F,1
G	E,1	G,1

   [16]

8. (a) Construct an ASM chart for a decimal system that counts the number of people in a room. People enter the room from one door, with a photocell that changes a signal x from 1 to 0, when the light is interpreted. They leave the room from a second door, with a similar photocell with a signal y. Both x and y are synchronized with a clock but they may stay on or off for more than one clock pulse period. The data processor subsystem consists of an up down counter with a display of its contents.

   (b) Design a four bit counter with synchronous clear with a diagram specified in the data processor

   [8+8]

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