Code No: RR310201 **Set No. 1**

III B.Tech I Semester Regular Examinations, November 2006
COMPUTER ORGANIZATION
(Common to Electrical & Electronic Engineering, Electronics & Communication Engineering, Electronics & Instrumentation Engineering, Electronics & Telematics and Instrumentation & Control Engineering)

Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
All Questions carry equal marks

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1. (a) List the types of transfers supported by interconnection structure.
   (b) Discuss the reasons for undermining bus performance
   (c) Explain various bus configuration examples. [5+5+6]
2. (a) Explain how floating point division is done?
   (b) Explain the addition of binary numbers in one's complement notation. [10+6]
3. (a) List the instruction formats used on the PDP-11.
   (b) Draw and explain Pentium instruction format. [8+8]
4. (a) Differentiate between interrupts and exceptions.
   (b) What do you mean by interrupt vector table?
   (c) Write about Pentium exception and interrupt vector table. [5+5+6]
5. (a) Explain the cache execution of a read operation with a neat diagram
   (b) Explain look-aside system organization for caches. [8+8]
6. (a) Explain about the magnetic disk principles along with it's advantages.
   (b) Discuss the format of a disk address word.
   (c) Discuss about disk operations. [6+5+5]
7. (a) Discuss about I/O channel architecture.
   (b) Discuss about I/O addressing in 8086.
   (c) Discuss the salient features of laser printer [6+6+4]
8. (a) Why special handling is required for branch instruction in a pipelined processor. Explain with examples.
   (b) How would you determine the number of pipeline stages in a pipelined processor [10+6]

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Code No: RR310201 **Set No. 2**

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Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
All Questions carry equal marks

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1. (a) How mandatory signal lines for PCI are functionally grouped
   (b) Explain typical desktop system using PCI configuration. [8+8]
2. Write an algorithm to find all allowable weights for a "weighted BCD code". Assume that all weights are positive numbers [16]
3. Explain various characteristics of machine instructions in detail [16]
4. (a) List and describe floating-point arithmetic instructions of Motorola 88000 instruction set.
   (b) Discuss about architecture of Motorola 88000. [8+8]
5. (a) Explain the cache execution of a read operation with a neat diagram
   (b) Explain look-aside system organization for caches. [8+8]
6. (a) Discuss about power PC interrupt structure.
   (b) Explain various registers in a DMA interface with their purpose. [8+8]
7. (a) Discuss about I/O channel architecture.
   (b) Discuss about I/O addressing in 8086.
   (c) Discuss the salient features of laser printer [6+6+4]
8. (a) Explain the following terms.
      i. Read miss
      ii. Read hit
      iii. Write miss
      iv. Write hit
   (b) Discuss different approaches to vector computation [8+8]

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Code No: RR310201 **Set No. 3**

III B.Tech I Semester Regular Examinations, November 2006
COMPUTER ORGANIZATION
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Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
All Questions carry equal marks

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1. (a) How optional signal lines for PCI are functionally grouped .
   (b) Explain typical server system using PCI configuration. [8+8]
2. (a) Explain about the arithmetic in excess - 3 code.
   (b) Discuss about normalized floating point representation [6+10]
3. (a) Describe various arithmetic and logical instruction set operations.
   (b) List CPU actions for various types of operations [8+8]
4. Elaborate on different types of registers in a register organization [16]
5. (a) Explain the principles of segmentation .
   (b) Discuss about address translation in segmentation.
   (c) What is hit ratio? [6+6+4]
6. (a) Elaborate about purpose and organization of data on magnetic tap
   (b) Differentiate between magnetic-disk and magnetic-tape systems
   (c) Discuss the technology used for CD-ROM systems [6+4+6]
7. (a) Explain the principles and working of dot matrix printers.
   (b) Differentiate between different types of printers. [8+8]
8. (a) Explain different types of parallel processors.
   (b) What do you mean by compound instruction? Give examples
   (c) Elaborate on registers of the IBM3090 vector facility. [4+6+6]

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Code No: RR310201 **Set No. 4**

III B.Tech I Semester Regular Examinations, November 2006
COMPUTER ORGANIZATION
(Common to Electrical & Electronic Engineering, Electronics & Communication Engineering, Electronics & Instrumentation Engineering, Electronics & Telematics and Instrumentation & Control Engineering)

Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
All Questions carry equal marks

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1. Describe all optional PCI signal lines with designation and type. [16]
2. Write an algorithm to add binary numbers represented in normalized floating point mode with base 2 for exponent. [16]
3. (a) Discuss various aspects of instruction set design.
   (b) Explain about various types of data on which machine instructions operate. [10+6]
4. (a) Differentiate between large register file versus cache.
   (b) Discuss how compiler based register optimization is done.
   (c) Explain various characteristics of reduced instruction set architectures. [6+6+4]
5. (a) Differentiate between single versus two-level caches.
   (b) Elaborate on Pentium Cache Organization. [8+8]
6. (a) What is 'data striping' ?
   (b) Discuss about the recent disk system developments.
   (c) Explain the control command operations enabled by magnetic tape drive controller. Also explain about cartridge tape system. [4+4+8]
7. (a) Discuss about I/O channel architecture.
   (b) Discuss about I/O addressing in 8086.
   (c) Discuss the salient features of laser printer [6+6+4]
8. (a) Give a summary of arithmetic and logical operations that are defined for the vector architecture.
   (b) What is cache coherence problem. Discuss about different cache coherance approches. [8+8]

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