Code No: RR311903 **Set No. 1**

III B.Tech I Semester Regular Examinations, November 2006
MICROPROCESSORS AND INTERFACING
(Electronics & Computer Engineering)

Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
All Questions carry equal marks

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1. 8086 processor do not provide memory indirect addressing mode. Show all possible ways to access a word from memory where the segment address is given in location 2000H:1000H and the offset is given in location 2000H:1002H. Give the instruction sequence for every addressing mode of 8086.? [16]

2. (a) Explain with example how a far procedure is declared as PUBLIC? Show how an external near procedure is called in main program?
   (b) Discuss the assembler directives with examples? [6+10]

3. Explain the following data transfer schemes.
   (a) Programmed I/O
   (b) Interrupted I/O
   (c) DMA [5+5+6]

4. (a) With neat layout, explain how a microprocessor can be used for data acquisition system using A/D converters and D/A converters?
   (b) Explain the transistor buffer circuit used to drive 7-segment LEDs? [10+6]

5. (a) A terminal is transmitting asynchronous serial data at 1200 bd. What is the bit time? Assuming 8 data bits, a parity bit and 1 stop bit how long does it take to transmit one character?
   (b) Draw necessary circuit to interface 8251 to an 8086 based system with an address 0C0H. Write the sequence of instructions to initialize 8251 for synchronous transmission? (Assume the necessary data) [8+8]

6. In an 8086 based system it is necessary to serve 64 IRQ's from different initiators. The allocated address space for 8259's is from 0700h to 070FH. Give the complete design by choosing the appropriate address locations in the above range? Give the initialization sequence for all 8259's with each IRQ activated in level triggered mode and the starting interrupt is type 40H? [16]

7. (a) Design the required logic to generate read, write control signals for memory and I/O in a target system using 8086 microprocessor? Generate bank select signals for even and odd address memory banks?
   (b) With the help of basic cell explain SRAM and DRAM? Discuss the advantages and disadvantages of the above memories? [8+8]

8. (a) Explain the internal RAM organization of 8051? Discuss how switching between register banks is possible? Give a sequence of instructions to switch from bank-0 to bank-2?

   (b) What is the use of SFR? List out the special function registers of 8051? [10+6]

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Code No: RR311903 **Set No. 2**

III B.Tech I Semester Regular Examinations, November 2006
MICROPROCESSORS AND INTERFACING
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Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
All Questions carry equal marks

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1. (a) What is the purpose of addressing mode? It is necessary to move a byte from location 5000H:0102H to 5000H:0050H. Give all possible methods using 8086 addressing modes?
   (b) Explain the use of Direction flag and Interrupt flag with examples? [10+6]

2. (a) Explain with example how a far procedure is declared as PUBLIC? Show how an external near procedure is called in main program?
   (b) Discuss the assembler directives with examples? [6+10]

3. Describe the function of the following pins in 8086 maximum mode of operation.
   (a) $\overline{TEST}$
   (b) RQ/GT_0 and RQ/GT_1
   (c) QS_0 & QS_1
   (d) S_0, S_1 , S_2 [2+4+4+6]

4. It is necessary to initialize interrupt for mode 1 operation of port-A as input and port-B as output in the same mode with the 8255 address map of 0400H to 0700H. Give the complete hard ware design to interface 8255 to 8086 processor with this address map? Write the instruction sequence for the initialization of 8255 in the above modes? Give the instruction sequence to change the operation modes of port A, port C lower-half and Port B to mode 0 input ports? [16]

5. (a) Draw the flowchart showing how synchronous serial data can be sent from a port line using software routine?
   (b) Draw the block diagram of 8237 and explain each block. [8+8]

6. In an 8086 based system it is necessary to serve 64 IRQ's from different initiators. The allocated address space for 8259's is from 0700h to 070FH. Give the complete design by choosing the appropriate address locations in the above range? Give the initialization sequence for all 8259's with each IRQ activated in level triggered mode and the starting interrupt is type 40H? [16]

7. (a) Explain the following terms with reference to DRAM
      i. Write cycle
      ii. Access time
      iii. Refresh

iv. Read cycle [4x2=8]

(b) Design the required logic to generate read, write control signals for memory and I/O in a target system using 8086 microprocessor? Generate bank select signals for even and odd address memory banks? [8]

8. Interface two 8255's to 8051 with starting address of 0FFF0H? Show the hardware design? Write the instruction sequence to initialize all ports of 8255?s as input ports in mode 0. [16]

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Code No: RR311903 **Set No. 3**

III B.Tech I Semester Regular Examinations, November 2006
MICROPROCESSORS AND INTERFACING
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Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
All Questions carry equal marks

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1. The register contents of 8086 is given below.

   CS=5000H, DS=8000H, SS=9000H, ES=7000H, SI=1000H, DI=2000H, BP=0008H, SP=0002H, AX=0000H, BX=5200H, CX=8000H, DX=2800H

   Calculate the effective address and physical address of the following instructions.

   (a) MOV AX, [BP+BX-24D]
   (b) ADD AX, ES:[SI]
   (c) PUSH CX
   (d) SUB AX, [DI]
   (e) MOVSB
   (f) CMP AX, [DI]
   (g) ADD DX, [DI+8D]
   (h) MUL AX, [SI+2D] [16]

2. (a) Explain in detail the coding template for 8086 MOV instruction? [8]
   (b) Write briefly about
      i. PUBLIC directive
      ii. EXTERN directive [4+4]

3. Describe the function of the following pins in 8086 maximum mode of operation.

   (a) $\overline{TEST}$
   (b) RQ/GT_0 and RQ/GT_1
   (c) QS_0 & QS_1
   (d) S_0, S_1 , S_2 [2+4+4+6]

4. Interface a 12-bit DAC to 8255 with an address map of 0C00H to 0C03H. The DAC provides output in the range of +5V to -5V. Write the instruction sequence.

   (a) For generating a square wave with a peak to peak voltage of 4V and the frequency will be selected from memory location 'F'.
   (b) For generating a triangular wave with a maximum voltage of +3V and a minimum of -2V. [6+10]

5. (a) With a neat sketch explain 8237 DMA controller and its operation? [8]
   (b) How do we connect RS-232C equipment
      i. To data terminal type devices?
      ii. To serial port of SDK ?86, RS-232C connection? [4+4]

6. (a) Draw the block diagram of 8259 and explain each block? Discuss the salient features of 8259?
   (b) What is the address map of interrupt address vector table? How many interrupts that this table can serve? [11+5]

7. In an SDK-86 kit 64KB SRAM and 32KB EPROM is provided on system and provision for expansion of another 64KB SRAM is given. The on system SRAM address map is from 00000H to 0FFFFH and that of EPROM is from F8000H to FFFFFH. The expansion slot address map is from 80000H to 8FFFFH. The size of SRAM chip is 32KB. EPROM chip size is 16KB. Give the complete memory interface and also the address map for individual chips? [16]

8. (a) Discuss the advantages of microcontroller based systems over microprocessor based systems?
   (b) With a neat sketch discuss the internal architecture of 8051? [6+10]

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Code No: RR311903 **Set No. 4**

III B.Tech I Semester Regular Examinations, November 2006
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Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
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1. (a) Give the 8085 compatible flags of 8086 processors? Discuss the design of each flag?
   (b) List out segmentation resisters of 8086? Explain how 8086 provides 1 MB memory address space using the segment registers? What is the purpose of extra segment? [8+8]

2. (a) Explain with example how a far procedure is declared as PUBLIC? Show how an external near procedure is called in main program?
   (b) Discuss the assembler directives with examples? [6+10]

3. (a) Explain how an 8086 enters into Wait State? How many wait states can be inserted in a machine cycle?
   (b) What is the difference between system bus cycle and bus idle cycle? Draw the timing diagram of bus idle cycle? [6+10]

4. Interface a stepper motor with 8-step input sequence to 8086 based system and write the instruction sequence to move the stepper motor 20 steps in clockwise and 12 steps in anti-clockwise direction. [8+8]

5. (a) Discuss Overrun error and Framing error with reference to 8251?
   (b) Discuss the mode instruction format of 8251 for synchronous and asynchronous mode of operation?
   (c) Explain single transfer mode and block transfer mode of 8237? [5+5+6]

6. (a) Discuss the five types of interrupts supported by 8086 and their function?
   (b) Write about interrupt vectors? How many bytes of memory do an interrupt vector requires?
   (c) Address 0100H in the interrupt vector table contains 7000H and address 0102H contains 0040H.
      i. To what interrupt type do these 4 locations correspond?
      ii. What is the starting address for the interrupt service routine? [9+3+4]

7. In an SDK-86 kit 64KB SRAM and 32KB EPROM is provided on system and provision for expansion of another 64KB SRAM is given. The on system SRAM address map is from 00000H to 0FFFFH and that of EPROM is from F8000H to FFFFFH. The expansion slot address map is from 80000H to 8FFFFH. The size of SRAM chip is 32KB. EPROM chip size is 16KB. Give the complete memory interface and also the address map for individual chips? [16]

8. (a) Explain the internal RAM organization of 8051? Discuss how switching between register banks is possible? Give a sequence of instructions to switch from bank-0 to bank-2?

   (b) What is the use of SFR? List out the special function registers of 8051? [10+6]

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