Code No: RR310401 **Set No. 1**

III B.Tech I Semester Regular Examinations, November 2006
DIGITAL IC APPLICATIONS
(Electronics & Communication Engineering)

Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
All Questions carry equal marks

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1. (a) Design a CMOS transistor circuit that has the functional behaviour f (Z) = $\overline{A.(B+C)}$
   (b) Design a 4-input CMOS AND-OR-INVERT gate? Draw the logic diagram and function table? [8+8]
2. (a) Draw the circuit diagram of a two-input LS-TTL NOR gate and explain the functional behavior?
   (b) Mention the DC noise margin levels of ECL 10K family? [8+8]
3. Design the logic circuit and write a data-flow style VHDL program for the following functions?
   (a) F (P) = $\Pi_{A,B,C,D}$ (1,7,9,13,15)
   (b) F (Y) = $\Sigma_{A,B,C,D}$ (1,4,5,7,12,14,15) + d(3,11) [8+8]
4. A mechanical disk rotates in a circle in different positions. Two successive positions differ with an angle of 15^0 . Provide an encoding mechanism for every position of the disk? The disk in the mechanical system outputs this encoded information to detect the exact position. Design a decoder with an enable input to identify the position of the disk? [8+8=16]
5. (a) Design a full subtractor with logic gates and write VHDL data flow program for the implementation of the above subtractor?
   (b) Using the above subtractor design a 8-bit ripple subtractor and write the corresponding VHDL program? [8+8]
6. (a) Design an 8-bit synchronous binary counter with serial enable control?
   (b) Draw the logic diagram of 74×163 binary counter and explain its operation? [8+8]
7. (a) Draw the logic diagram of 74x194 and explain the operation?
   (b) Design a serial binary adder? Develop the VHDL program for simulating serial binary adder? [8+8]
8. (a) Explain the internal structure of 64Kx1 DRAM? With the help of timing waveforms discuss DRAM access?
   (b) Explain XC4000 programmable interconnect structure? [8+8]

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Code No: RR310401 **Set No. 2**

III B.Tech I Semester Regular Examinations, November 2006
DIGITAL IC APPLICATIONS
(Electronics & Communication Engineering)

Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
All Questions carry equal marks

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1. (a) Explain the effect of floating inputs on CMOS gate?
   (b) Explain how a CMOS device is destroyed?
   (c) What is the difference between transmission time and propagation delay? Explain these two parameters with reference to CMOS logic? [4+4+8]
2. (a) Design a TTL three-state NAND gate and explain the operation with the help of function table? [8]
   (b) Explain the following terms with reference to TTL gate?
      i. Logic levels
      ii. DC Noise margin
      iii. Low-state unit load
      iv. High-state fanout [4+4]
3. Design the logic circuit and write a data-flow style VHDL program for the following functions?
   (a) F (Q) = $\Sigma_{A,B,C,D}$ (0,2,5,7,8,10,13,15) + d(11)
   (b) F (R) = $\Pi_{A,B,C,D}$ (1,4,5,7,9,13,15) [8+8]
4. (a) Using two 74×138 decoders design a 4 to 16 decoder?
   (b) Design a 16-bit comparator using 74×85s? [8+8]
5. Design a combinational logic circuit that counts the number of ones in a 24-bit register? Write a VHDL program for the above implementation? [8+8]
6. (a) Design a conversion circuit to convert a D flip-flop to J-K flip-flop? Write data-flow style VHDL program?
   (b) Design a 4-bit binary synchronous counter using 74×74? Write VHDL program for this logic? [8+8]
7. (a) Design an 8-bit serial-in and parallel-out shift register with flip-flops? Explain the operation with the help of timing waveforms?
   (b) Write VHDL data-flow program for the above shift-register? [8+8]
8. (a) Discuss the operation of IOB in XC4000 FPGA with a neat sketch?
   (b) Realize the logic function performed by 74x381 with ROM? [8+8]

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Code No: RR310401 **Set No. 3**

III B.Tech I Semester Regular Examinations, November 2006
DIGITAL IC APPLICATIONS
(Electronics & Communication Engineering)

Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
All Questions carry equal marks

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1. (a) What are the parameters that are necessary to define the electrical characteristics of CMOS circuits? Mention the typical values of a CMOS NAND gate?
   (b) Design a 4-input CMOS AND-OR-INVERT gate? Draw the logic diagram and function table? [8+8]

2. (a) Explain the difference in program structure of VHDL and any other procedural language? Give an example?
   (b) Explain sinking current and sourcing current of TTL output? Which of the above parameters decide the fanout and how? [8+8]

3. (a) What is the importance of time dimension in VHDL and explain its function?
   (b) Design the logic circuit and write a data-flow style VHDL program for the following function?
   F (X) = $\Sigma_{A,B,C,D}$ (0,1,3,5,14) + d(8,15) [8+8]

4. (a) Realize the following expression using 74x151 IC?
   f (X) = $\bar{A}BC + A\bar{B}C + AB\bar{C}$
   (b) Design a 16-bit comparator using 74×85 Ics? [8+8]

5. (a) Show the logic diagram of 74×283 binary adder? Explain the principle of generating sum and carry at every stage using the logic diagram? [4+4]
   (b) Design a 24-bit group ripple adder using 74×283 Ics? [8]

6. (a) Distinguish between latch and flip-flop? Show the logic diagram for both? Explain the operation with the help of function table? [4+4]
   (b) Design a conversion circuit to convert a T flip-flop to J-K flip-flop? [8]

7. (a) What is the difference between ring counter and Johnson ring counter? Design a self-correcting 4-bit, 4-state ring counter with a single circulating 0 using 74x194?
   (b) Define clock skew? Explain how clock skew leads to incorrect outputs in synchronous circuits? Design one logic circuit that minimizes clock skew? [8+8]

8. (a) Explain the internal structure of 64Kx1 DRAM? With the help of timing waveforms discuss DRAM access?

(b) Explain XC4000 programmable interconnect structure? [8+8]

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Code No: RR310401 **Set No. 4**

III B.Tech I Semester Regular Examinations, November 2006
DIGITAL IC APPLICATIONS
(Electronics & Communication Engineering)

Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
All Questions carry equal marks

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1. (a) Explain how to estimate sinking current for low output and sourcing current for high output of CMOS gate?
   (b) Analyze the fall time of CMOS inverter output with R_L = 1K?, V_L = 2.5V and C_L = 100PF. Assume VL as stable state voltage. [8+8]
2. (a) Draw the circuit diagram of basic CMS gate and explain the operation?
   (b) Design a transistor circuit of 2-input ECL NOR gate? Explain the operation with the help of function table? [8+8]
3. (a) Explain data-flow design elements of VHDL? [8]
   (b) Write a data-flow style VHDL program for the following functions?
   F(S) = A $\oplus$B$\oplus C_I$
   F(C_O) = $AB + AC_I + BC_I$ [4+4]
4. (a) Using two 74×138 decoders design a 4 to 16 decoder?
   (b) Write a data flow style VHDL program for the above design? [8+8]
5. Draw the logic diagram of 74×283 IC and explain the operation? Write data flow VHDL program for this IC? [4+4+8]
6. (a) Design a 4-bit binary synchronous counter using 74×74? Write VHDL program for this logic?
   (b) Design a modulo-60 counter using 74×163 ICs? [8+8]
7. (a) Design an 8-bit parallel-in and parallel-out shift register and explain the operation?
   (b) Write data-flow style VHDL program for the above circuit? [8+8]
8. (a) With the help of timing waveforms, explain read and write operations of static SRAM?
   (b) With a neat sketch, explain the general architecture of FPGA chip? What is the importance of configurable logic block? [8+8]

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