MAHATMA GANDHI INSTITUTE OF TECHNOLOGY (Autonomous)
M.Tech. in Digital Electronics and Communication Engineering
Scheme of Instruction and Examination
(Choice Based Credit System)

With effect from the academic year 2022-23

I Semester

S.No.	Course Code	Course Title	Instruction Hours Per Week			Examination Max. Marks		Duration of SEE in Hours	Credits
			L	T	P/D	CIE	SEE		
1	EC101PC	Digital System Design with FPGA	3	0	0	40	60	3	3
2	EC102PC	Advanced Wireless Communications	3	0	0	40	60	3	3
3	EC11XPE	**Professional Elective – I**	3	0	0	40	60	3	3
4	EC11XPE	**Professional Elective – II**	3	0	0	40	60	3	3
5	EC101MC	Research Methodology & Intellectual Property Rights	2	0	0	40	60	3	2
6	AC10XHS	Audit Course – I	2	0	0	40	60	3	0
7	EC151PC	Digital System Design Laboratory	0	0	4	40	60	3	2
8	EC152PC	Wireless Communications and Networks Laboratory	0	0	4	40	60	3	2
		Total Hours/Marks/Credits	**16**	**0**	**8**	**320**	**480**		**18**

II Semester

S.No.	Course Code	Course Title	Instruction Hours Per Week			Examination Max. Marks		Duration of SEE in Hours	Credits
			L	T	P/D	CIE	SEE		
1	EC201PC	ARM Microcontrollers and Programmable Digital Signal Processors	3	0	0	40	60	3	3
2	EC202PC	Advanced Communications and Networks	3	0	0	40	60	3	3
3	EC21XPE	**Professional Elective – III**	3	0	0	40	60	3	3
4	EC21XPE	**Professional Elective – IV**	3	0	0	40	60	3	3
5	AC20XHS	Audit Course – II	2	0	0	40	60	3	0
6	EC251PC	ARM Microcontrollers and Programmable Digital Signal Processors Laboratory	0	0	4	40	60	3	2
7	EC252PC	Advanced Communications and Networks Laboratory	0	0	4	40	60	3	2
8	EC253PC	Mini project with Seminar	0	0	4	100	-	-	2
		Total Hours/Marks/Credits	**14**	**0**	**12**	**380**	**420**		**18**

L: Lecture **T**: Tutorial **D**: Drawing **P**: Practical **CIE** - Continuous Internal Evaluation **SEE** - Semester End Examination

III Semester

S.No.	Course Code	Course Title	Instruction			Examination			Credits
			Hours Per Week			Max. Marks		Duration of SEE in Hours	
			L	T	P/D	CIE	SEE		
1	EC31XPE	Professional Elective – V	3	0	0	40	60	3	3
2	EC32XOE	Open Elective	3	0	0	40	60	3	3
3	EC351PC	Dissertation Stage-II	0	0	12	100	-	-	6
Total Hours/Marks/Credits			**6**	**0**	**12**	**180**	**120**		**12**

IV Semester

S.No.	Course Code	Course Title	Instruction			Examination			Credits
			Hours Per Week			Max. Marks		Duration of SEE in Hours	
			L	T	P	CIE	SEE		
1	EC451PC	Dissertation Stage-III	0	0	12	100	--	-	6
2	EC452PC	Dissertation VIVA VOCE	0	0	28	--	100	-	14
Total Hours/Marks/Credits			**0**	**0**	**40**	**100**	**100**		**20**

L: Lecture **T**: Tutorial **D**: Drawing **P**: Practical **CIE** - Continuous Internal Evaluation **SEE** - Semester End Examination

Grand Total of Credits

Semester	I	II	III	IV	Total Credits
Credits	18	18	12	20	68

Professional Elective

Professional Elective – I
EC111PE: CMOS Digital VLSI Design
EC112PE: Advanced Computer Architecture
EC113PE: Real Time Operating Systems

Professional Elective – II
EC114PE: Coding Theory and Techniques
EC115PE: Mobile Computing
EC116PE: Design of Fault Tolerant Systems

Professional Elective – III
EC211PE: Embedded Systems Design
EC212PE: Low power CMOS VLSI Design
EC213PE: Computer Vision

Professional Elective – IV
EC214PE: Deep Learning
EC215PE: Pattern Recognition and Machine Learning
EC216PE: Ad-hoc & Wireless Sensor Networks

Professional Elective-V
EC311PE: MIMO Systems
EC312PE: System on Chip Architecture
EC313PE: Embedded Networking

Audit Courses

Audit Course-I
AC101HS**:** English for Research Paper Writing
AC102HS: Disaster Management
AC103HS: Sanskrit for Technical Knowledge
AC104HS: Value Education
Audit Course-II
AC201HS: Constitution of India
AC202HS: Pedagogy Studies
AC203HS: Stress Management by Yoga
AC204HS: Personality Development through Life Enlightenment Skills

List of Open Electives offered by Department of Electronics and Communication Engineering to other branches:
Open Elective
EC321OE: System on Chip Architecture
EC322OE: Cognitive Radio
EC323OE: IoT and Its Applications

L	T	P	C
3	0	0	3

M.Tech. in Digital Electronics and Communication Engineering
I Semester Syllabus
EC101PC: Digital System Design with FPGA

Course Objectives

The objectives of this course are to make the student

1. To understand the Basics Modeling Concepts of Verilog HDL.
2. To provide an Overview of System Design approach using Programmable Logic Devices.
3. To learn the commercially available and techniques of CPLDs & FPGAs.
4. To get exposed to the various architectural features of CPLDs and FPGAs.
5. To implement the Sequential Circuits on CPLDs and FPGAs using CAD Tools.
6. To provide extended knowledge of Digital Logic Circuits in the Form of State Table and State Model Approach.

Course Outcomes

At the end of this course, students will be able to

1. Apply the Verilog HDL Concepts for Digital Circuits.
2. Narrate the Concepts of ROMs, PALs, PLAs CPLDs and FPGAs.
3. Design and Develop Different Sequential Circuits.
4. Implement Sequential Circuit Design using FPGAs/CPLDs.
5. Analyze the Clocked Sequential Circuits with State Graphs and State Tables.

Course Articulation Matrix

COs	PO1	PO2	PO3	PO4	PO5	PO6
CO1	3	-	2	2	3	-
CO2	2	-	-	3	3	1
CO3	3	-	-	3	2	-
CO4	3	-	-	3	2	-
CO5	1	-	2	2	2	-

Unit - I

Verilog HDL Coding Style: Overview of Digital Design with Verilog HDL, Hierarchical Modeling Concepts, Basic Concepts of Modules and Ports, Gate Level Modeling, Dataflow Modeling, Behavioral Modeling, Tasks and Functions, Useful Modeling Techniques.

Unit - II

Programmable Logic Devices: The Concept of Programmable Logic Devices, SPLDs, PAL Devices, PLA Devices, GAL Devices, CPLD Architecture, Xilinx CPLDs, Altera CPLDs, FPGAs- FPGA Architecture, Vertex CLB and Slice- Stratix LAB and ALM-RAM Blocks, DSP Blocks, Clock Management, I/O Standards, Additional Features.

Unit - III

FPGAs/CPLDs: FPGAs/CPLDs Programming Technologies, Commercially Available FPGAs, Xilinx's Vertex and Spartan, Actel's FPGA, Altera's FPGAs/CPLDs.

Unit - IV

Sequential Circuit Design: Design Procedure for Sequential Circuits, Design Example, Code Converter, Design of Iterative Circuits, Design of a Comparator, Design of Sequential Circuits using ROMs and PLAs, Sequential Circuit Design using CPLDs, Sequential Circuit Design using FPGAs, Simulation and Testing of Sequential Circuits, Overview of Computer aided Design.

Unit - V

Analysis and Derivation of Clocked Sequential Circuits with State Graphs and Tables: A Sequential Parity Checker, Analysis by Signal Tracing and Timing Charts-State Tables and Graphs General Models for Sequential Circuits, Design of a Sequence Detector, more Complex Design Problems, Guidelines for Construction of State Graphs, Serial Data Code Conversion, Alphanumeric State Graph Notation.

Suggested Readings:

1. Volnei A. Pedroni, "Digital Electronics and Design with VHDL"- Elsevier publications 1st Edition ,2008.
2. John V. Old Field, Richard C. Dorf, "Field Programmable Gate Arrays", Wiley, 2008.
3. Charles H. Roth, Jr. "Fundamentals of Logic Design" -Enhanced 7th Edition 2020.

Reference Books:

1. Samir Palnitkar, "Verilog HDL, A Guide to Digital Design and Synthesis" Prentice Hall, 2 nd Edition, 2003.
2. S. Ramachandran, "Digital VLSI System Design", A Design Manual for Implementation of Projects on FPGAs and ASICs Using Verilog" Springer Publication, 1st Edition, 2007.
3. Wayne Wolf, "FPGA Based System Design", Prentices Hall Modern Semiconductor Design Series 2004.
4. Digital System Design using Programmable Logic Devices- Parag K. Lala, BS Publications 2003.

L	T	P	C
3	0	0	3

M.Tech. in Digital Electronics and Communication Engineering
I Semester Syllabus
EC102PC: Advanced Wireless Communications

Course Objectives

The objectives of this course are to make the student

1. Discuss about the cellular system fundamentals and Handoff Strategies.
2. Understand the impact of fading effects on the performance communication system.
3. Discuss and derive the capacity of AWGN and MIMO channels.
4. Discuss fundamentals of Equalization in a communication Receiver.
5. Understand the basics Software defined radio.

Course Outcomes

At the end of this course, students will be able to

1. Introduce the concepts and techniques associated with Wireless Cellular Communication systems.
2. Summarize and analyze fading effects and diversity techniques.
3. Illustrate and evaluate the capacity of AWGN and MIMO channels.
4. To distinguish the equalization techniques.
5. Analyze and design CDMA and OFDM system functioning.
6. Illustrate transceiver elements of Software defined radio.

Course Articulation Matrix

COs	PO1	PO2	PO3	PO4	PO5	PO6
CO1	-	-	2	2	2	-
CO2	2	-	3	2	2	-
CO3	-	-	2	1	2	-
CO4	-	-	2	2	2	2
CO5	2	-	2	3	3	-
CO6	-	-	2	2	2	2

Unit - I

Cellular Communication Fundamentals: Introduction, Frequency Reuse, Channel Assignment Strategies, Handoff Strategies, Interference and system capacity, Trunking and Grade of Service, Improving Coverage & Capacity in Cellular Systems–cell splitting, sectoring, Comparison of 1G, 2G, 3G & 4G.

Unit - II

Fading Channels And Diversity Techniques: Wireless channels – Error/Outage probability over fading channels – Diversity techniques – Channel coding as a means of time diversity – Multiple antennas in wireless communications.

Unit - III

Capacity & Information Rates Of Mimo Channels: Capacity and Information rates of noisy, AWGN and fading channels – Capacity of MIMO channels – Capacity of non-coherent MIMO channels – Constrained signaling for MIMO communications.

Unit - IV

Equalization: Fundamentals of Equalization, Training a Generic Adaptive Equalizer, Equalizers in a communications receiver, classification of equalization techniques. Linear Equalizers, Nonlinear Equalization, Algorithms for adaptive equalization.

CDMA: CDMA Digital Cellular Standard (IS-95), Forward CDMA Channel, Reverse CDMA Channel.

OFDM-Basic principles, Block diagram and Mathematical representation.

Unit - V

Introduction to Software-defined Radios: Need for Software-defined Radio, Characteristics and benefits of Software-defined Radio - Design Principles of Software-defined Radio, RF Implementation issues- The Purpose of RF Front – End, Dynamic Range- The Principal Challenge of Receiver Design – RF Receiver Front End Topologies- Enhanced Flexibility of the RF Chain with Software-defined Radios - Importance of the Components to Overall Performance- Transmitter Architectures and Their Issues- Noise and Distortion in the RF Chain, ADC and DAC Distortion.

Suggested Readings:

1. T.S.Rappaport, "Wireless Communications, Principles and Practice", 2nd edition, PHI, 2010.
2. William C.Y.Lee, "Mobile Cellular Telecommunications Analog and Digital Systems", 2nd edition, TMH, 2006.
3. UpenaDalal, "Wireless Communication", Oxford University Press, 8th Impression, 2015.
4. Aditya K Jagannatham, "Principles of Modern Wireless Communication Systems Theory and Practice", McGraw Hill India, 2015.
5. Markus Dillinger, Kambiz Madani, "Software Defined Radio Architecture System and Functions", WILEY 2003

Reference Books:

1. KavehPahLaven and P. Krishna Murthy," Principles of Wireless Networks-, Pearson Education, 2006.
2. V.K.Garg, J.E.Wilkes, "Principle and Application of GSM", Pearson Education, 5th edition, 2008.
3. V.K.Garg, "IS-95 CDMA & CDMA 2000", Pearson Education, 4th edition, 2009.
4. Mischa Schwartz, "Mobile wireless communications", Cambridge university press, 2013.
5. Walter Tuttle Bee, "Software Defined Radio: Enabling Technologies", 2002, Wiley Publications.

L	T	P	C
3	0	0	3

M.Tech. in Digital Electronics and Communication Engineering
I Semester Syllabus
Professional Elective – I
EC111PE: CMOS Digital VLSI Design

Course Objectives

1. To Understand the Basic Concepts of MOS Structure.
2. To Demonstrate the General Characteristics of MOS Transistor and CMOS Inverter.
3. To Estimate the Quality Metrics of a Digital Design.
4. To Design and Develop Combinational and Sequential Circuits.

Course Outcomes

After completion of the course the student should be able to

1. Recall the Concepts of Basic MOS Structure and its Static Behavior.
2. Explain the Quality Metrics of a Digital Design.
3. Discuss Physical Design flow and Advanced Technologies.
4. Design Different Types of Logic Gates using CMOS Inverter and analyze their Transfer Characteristics.
5. Design Combinational, Sequential and Memory circuits and Applying the Knowledge of Digital Design, to Build Complex Digital Circuits.

Course Articulation Matrix

COs	PO1	PO2	PO3	PO4	PO5	PO6
CO1	2	-	2	2	3	1
CO2	2	-	2	2	2	2
CO3	-	-	3	3	2	2
CO4	-	-	2	2	3	2
CO5	2	-	2	3	2	2

Unit - I

Review: Basic MOS structure and its static behavior.

Quality Metrics of a Digital Design: Cost, Functionality, Robustness, Power, and Delay, MOS Transistor Basic, MOS Parasitic & SPICE Model; wire delay models of MOS transistors.

Unit - II

CMOS Inverter: Static CMOS inverter, switching threshold and noise margin concepts and their evaluation, Dynamic behavior, Power consumption and Analyzing Power Consumption using SPICE

Unit - III

Combinational Logic: Static CMOS design, Logic effort, Ratioed logic, Pass transistor logic, Dynamic logic, Speed and power dissipation in dynamic logic, Cascading dynamic gates, CMOS transmission gate logic.

Unit - IV

Sequential Logic: Static latches and registers, Bi-stability principle, MUX based latches, Static SR flip-flops, Master-slave edge-triggered register, Dynamic latches and registers, Concept of pipelining, Pulse registers, and Non-Bi stable sequential circuit. Advanced Technologies: Giga-scale dilemma, Short channel effects, High–k, Metal Gate Technology, FinFET and TFET.

Unit - V

Physical Design Flow: Floor planning, Placement, Routing, CTS, Power analysis and IR drop estimation-static and dynamic, ESD protection-human body model, Machine model. Designing Memory & Array structures: SRAM and DRAM Memory Core - memory peripheral circuitry - Memory reliability and yield - Power dissipation in memories.

Suggested Readings:

1. J.P.Rabaey, A.P.Chandrakaran, B.Nikolic, "Digital Integrated Circuits: A design Perspective", Prentice Hall Electronics & VLSI series, 2nd Edition, 2008.
2. Pucknell, D.A. and Eshraghian, K., "Basic VLSI Design", PHI, 3rd Edition, 2012.

Reference Books:

1. Baker, Li, Boyce, "CMOS Circuit Design, Layout, and Simulation", 2nd Edition, Wiley.
2. R. J. Baker, "CMOS circuit Design, Layout and Simulation", IEEE Inc., 2008.
3. Kang. S and Leblebici .Y, "CMOS Digital Integrated Circuits, Analysis and Design", 3 rd Edition, TMH.

L	T	P	C
3	0	0	3

M.Tech. in Digital Electronics and Communication Engineering
I Semester Syllabus
Professional Elective – I
EC112PE: Advanced Computer Architecture

Course Objectives

Students from other engineering background to get familiarize with large scale integration technology.
1. To discuss about the computer architecture with the underlying design principles.
2. To understand the impact of pipelining and parallel processing on computer performance.
3. To study the methodology of processor and control design.
4. To describe memory organization, system organization, and parallel processing.

Course Outcomes

At the end of this course, students will be able to
1. Study the basics of parallelism, pipelining concepts, and pipeline architecture challenges.
2. Discuss the issues in vector and array processors.
3. Analyze the high performance scalable multi-threaded and multiprocessor systems.
4. Explain different parallel algorithms for multiprocessors systems based on performance.
5. Recognize various memory contention and different arbitration techniques used in multiprocessors systems.
6. Illustrate various synchronization techniques for parallel programming interface.

Course Articulation Matrix

COs	PO1	PO2	PO3	PO4	PO5	PO6
CO1	-	-	2	3	3	2
CO2	1	-	2	2	3	2
CO3	2	-	3	2	3	2
CO4	2	2	3	2	3	-
CO5	-	-	2	3	2	2
CO6	2	-	2	3	2	-

Unit - I

Parallel Processing and Pipelining Processing: Architectural Classification, Applications of Parallel Processing, Instruction Level Parallelism and Thread Level Parallelism, Explicitly Parallel Instruction Computing (EPIC) Architecture.

Unit - II

Pipeline Architecture: Principles and Implementation of Pipelining, Classification of Pipelining Processors, Design aspect of Arithmetic and Instruction Pipelining, Pipelining Hazards and Resolving Techniques, Data buffering techniques, Advanced Pipelining Techniques, Software Pipelining, VLIW (Very Long Instruction Word) processor.

Unit - III

Vector and Array Processor: Issues in Vector Processing, Vector Performance Modeling, SIMD Computer Organization, Static Vs Dynamic Network, Parallel Algorithms for Array Processors - Matrix Multiplication.

Unit IV

Multiprocessor Architecture: Loosely and Tightly Coupled Multiprocessors, Inter Processor Communication Network, Time Shared Bus, Multiport Memory Model, Memory Contention and Arbitration Techniques, Cache Coherency and Bus Snooping, Massively Parallel Processors (MPP).

Multithreaded Architecture: Multithreaded Processors, Latency Hiding Techniques, Principles of Multithreading, Issues and Solutions, Parallel Programming Techniques-Message Passing Program Development.

Unit - V

Parallel Algorithms for Multiprocessors: Classification and Performance of Parallel Algorithms, Operating Systems for Multiprocessors Systems, Message Passing Libraries for Parallel Programming Interface, Parallel Virtual Machine (PVM) (in distributed memory system), and Message Passing Interfaces (MPI).

Suggested Readings:

1. Kai Hwang and Faye A. Briggs, "Computer Architecture and Parallel Processing", McGraw Hill Education, 1st Edition2012.
2. Kai Hwang, "Advanced Computer Architecture", McGraw Hill Education, 1993.

Reference Books:

1.John L. Hennessy and David A. Patterson, ".Computer Architecture: A Quantitative Approach", Elsevier, 5 th Edition, 2012.
2.William Stallings, "Computer Organization and Architecture, Designing for Performance", Prentice Hall, 6th edition, 2006.
3. Kai Hwang, "Scalable Parallel Computing", McGraw Hill Education, 1998.
4. Harold S. Stone "High-Performance Computer Architecture", Addison Wesley, 1993.

L	T	P	C
3	0	0	3

M.Tech. in Digital Electronics and Communication Engineering
I Semester Syllabus
Professional Elective – I
EC113PE: Real Time Operating Systems

Course Objectives

The objectives of this course are to make the student
1. Understand the Real time scheduling theory concept.
2. Experience on real time scheduler implementation applied to real time systems.
3. Skills necessary to develop software for embedded computer systems using a real-time operating system.
4. Basic knowledge of RT Linux, Micro C/OS-II, Vx Works, Embedded Linux, and Tiny OS.

Course Outcomes

By the end of the course, the students will be able to:
1. Explain the concepts of UNIX operating systems.
2. Contrast Concepts of real time operating systems with GPOS.
3. Define Objects services and IO subsystems.
4. Instantiating with Exceptions, Interrupts and Timer operations built in RTOS.
5. Compare various Real Time OS.
6. Illustrate case study of RT Linux, uC/OS-II, Vx Works, Embedded Linux.

Course Articulation Matrix

COs	PO1	PO2	PO3	PO4	PO5	PO6
CO1	-	-	2	2	3	-
CO2	2	-	2	3	3	-
CO3	-	-	2	2	3	-
CO4	-	-	3	2	3	2
CO5	-	-	2	3	2	1
CO6	2	2	3	2	2	1

Unit - I

Introduction: Introduction to UNIX/LINUX, Overview of Commands, File I/O,(open, create, close, lseek, read, write), Process Control (fork, vfork, exit, wait, waitpid, exec).

Unit - II

Real Time Operating Systems: Brief History of OS, Defining RTOS, The Scheduler, Objects, Services, Characteristics of RTOS, Defining a Task, asks States and Scheduling, Task Operations, Structure, Synchronization, Communication and Concurrency. Defining Semaphores, Operations and Use, Defining Message Queue, States, Content, Storage, Operations and Use

Unit - III

Objects, Services and I/O: Pipes, Event Registers, Signals, Other Building Blocks, Component Configuration, Basic I/O Concepts, I/O Subsystem

Unit - IV

Exceptions, Interrupts and Timers: Exceptions, Interrupts, Applications, Processing of Exceptions and Spurious Interrupts, Real Time Clocks, Programmable Timers, Timer Interrupt Service Routines (ISR), Soft Timers, Operations.

Unit - V

Case Studies of RTOS: RT Linux, MicroC/OS-II, Vx Works, Embedded Linux, and Tiny OS.

Suggested Readings:

1. Qing Li, "Real Time Concepts for Embedded Systems", Elsevier, 2011
2. Embedded Real Time Systems: Concepts, Design Programming, Black book, Dream techPress 1st Edition 2003.

Reference Books:

1. W. Richard Stevens, Stephan A. Rago, "Advanced UNIX Programming", Pearson, 2nd Edition, 2006.
2 .Dr. Craig Hollabaugh, "Embedded Linux: Hardware, Software and Interfacing", Pearson, 1st Edition, 2008.
3. Introduction to Embedded Systems - Shibu K.V, McGraw Hill, 2nd Edition 2016

L	T	P	C
3	0	0	3

M.Tech. in Digital Electronics and Communication Engineering
I Semester Syllabus
Professional Elective – II
EC114PE: Coding Theory and Techniques

Course Objectives

The objectives of this course are to make the student
1. To acquire the knowledge in measurement of information and errors.
2. To study the generation of various code methods.
3. To study the various application of codes.

Course Outcomes

On completion of this course student will be able to
1. Learning the measurement of information and errors.
2. Obtain knowledge in designing Linear Block Codes and Cyclic codes.
3. Construct tree and trellies diagrams for convolution codes.
4. Design the Turbo codes and Space time codes and also their applications.

Course Articulation Matrix

COs	PO1	PO2	PO3	PO4	PO5	PO6
CO1	2	-	2	2	3	1
CO2	-	-	2	2	3	2
CO3	2	-	2	3	2	2
CO4	-	-	2	3	2	2

Unit - I

Coding for Reliable Digital Transmission and storage: Mathematical model of Information, A Logarithmic Measure of Information, Average and Mutual Information and Entropy, Types of Errors, Error Control Strategies.
Linear Block Codes Introduction to Linear Block Codes, Syndrome and Error Detection, Minimum Distance of a Block code, Error-Detecting and Error-correcting Capabilities of a Block code, Standard array and Syndrome Decoding, Probability of an undetected error for Linear Codes over a BSC, Hamming Codes. Applications of Block codes for Error control in data storage system

Unit - II

Cyclic Codes: Description, Generator and Parity-check Matrices, Encoding, Syndrome Computation and Error Detection, Decoding, Cyclic Hamming Codes, Shortened cyclic codes, Error-trapping decoding for cyclic codes, Majority logic decoding for cyclic codes.

Unit - III

Convolutional Codes: Encoding of Convolutional Codes, Structural and Distance Properties, maximum likelihood decoding, Sequential decoding, Majority- logic decoding of Convolution codes. Application of Viterbi Decoding and Sequential Decoding, Applications of Convolutional codes in ARQ system.

Unit - I V

Turbo Codes: LDPC Codes- Codes based on sparse graphs, Decoding for binary erasure channel, Log-likelihood algebra, Brief propagation, Product codes, Iterative decoding of product codes, Concatenated convolutional codes- Parallel concatenation, The UMTS Turbo code, Serial concatenation, Parallel concatenation, Turbo decoding

Unit - V

Space-Time Codes: Introduction, Digital modulation schemes, Diversity, Orthogonal space- Time Block codes, Alamouti‟s schemes, Extension to more than Two Transmit Antennas, Simulation Results, Spatial Multiplexing: General Concept, Iterative APP Preprocessing and Per-layer Decoding, Linear Multilayer Detection, Original BLAST Detection, QL Decomposition and Interface Cancellation, Performance of Multi – Layer Detection Schemes, Unified Description by Linear Dispersion Codes.

Suggested Readings:

1. Error Control Coding- Fundamentals and Applications –Shu Lin, Daniel J. Costello, Jr, Prentice Hall, Inc.
2. Error Correcting Coding Theory-Man Young Rhee, McGraw-Hill, 1989.

Reference Books:

1. Bernard Sklar, Digital Communications-Fundamental and Application, PE.
2. Proakis John .G, Digital Communications, 5th ed. TMH, 2008.
3. Todd K. Moon, Error Correction Coding – Mathematical Methods and Algorithms, Wiley India, 2006.
4. Ranjan Bose, Information Theory, Coding and Cryptography, 2nd Edition, TMH, 2009.

L	T	P	C
3	0	0	3

M.Tech. in Digital Electronics and Communication Engineering
I Semester Syllabus
Professional Elective – II
EC115PE: Mobile Computing

Prerequisite: Computer Networks, Computer Organization and architecture.

Course Objectives

The objectives of the course Mobile Computing are
1. To learn the fundamental technologies that help in the networking of wireless devices.
2. To study the cellular architectures of GSM, GPRS, SMS.
3. To have an exposure about emerging technologies like Blue tooth, WiMAX etc.
4. To know the Network, Transport functionalities of Mobile Communication.
5. To impart knowledge about Mobile Application Development using Palm OS, Symbian OS, J2ME etc.

Course Outcomes

After completion of the course students should be able to:
1. Articulate the basics of Mobile Computing and Communication standards.
2. Describe Mobile Communication and Computing Architectures.
3. Demonstrate the knowledge of various platforms like Palm OS, Symbian OS and Windows CE used for mobile devices.
4. Develop mobile applications using JAVA 2 micro edition (J2ME) technology.
5. Differentiate H.323, SIP and other protocols, frameworks for VoIP.
6. Analyze various security protocols and able to deal with security attacks in mobile environment.

Course Articulation Matrix

COs	PO1	PO2	PO3	PO4	PO5	PO6
CO1	2	-	2	3	2	2
CO2	-	-	-	3	2	-
CO3	-	-	2	-	3	-
CO4	-	-	3	-	-	2
CO5	2	-	-	2	2	-
CO6	2	-	-	3	2	-

Unit – I

Introduction to Mobile Computing Architecture: Mobile Computing, dialog control, networks, middleware and gateways, application and services, developing mobile computing applications, security in mobile computing, architecture for mobile computing, three tier architecture, design considerations for mobile computing, mobile computing through internet, making existing applications mobile-enabled.

Unit – II

Cellular Technologies – GSM, GPRS, CDMA AND 3G : Wireless Broadband, mobile IP, Internet protocol version 6 (IPv6), Java card, PLNM interfaces, GSM addresses and identifiers, network aspects in GSM, Mobile computing over SMS, Short Message Services (SMS), GPRS network architecture, GPRS network operations, data services in GPRS, applications for GPRS, limitations of GPRS, CDMA versus GSM, third generation networks, applications on 3G, Introduction to 4G & 5G Communications.

Unit – III

Wireless Application Protocol (WAP) and Wireless LAN: WAP, MMS, wireless LAN advantages, IEEE 802.11 standards, wireless LAN architecture, mobility in wireless LAN.

Intelligent and Internetworking: Introduction, fundamentals of call processing, intelligence in the networks, SS#7 signaling, IN Conceptual Model (INCM), Softswitch, programmable networks, technologies and interfaces for IN.

Unit – IV

Client Programming, PALM OS, SYMBIAN OS, WIN CE Architecture: Introduction, moving beyond the desktop, a peek under the hood: hardware overview, mobile phones, PDA, design constraints in applications for handheld devices, palm OS architecture, application development, Symbian OS architecture, Applications for Symbian, different flavors of windows CE, windows CE architecture.

J2ME: Java in the handset, the three prong approach to JAVA everywhere, JAVA 2 micro edition (J2ME) technology, programming for CLDC, MIDLet, Optional packages.

Unit – V

Voice Over Internet Protocol and Convergence:

Voice over IP, H.323 Framework for voice over IP, Session Initiation Protocol, Comparison between H.323 and SIP, Real Time protocols, Convergence Technologies, Call Routing, IP multimedia subsystem (IMS), Mobile VoIP.

Security Issues in Mobile Computing: Introduction, information security, security techniques and algorithms, security protocols, trust, security models, security frameworks for mobile environment.

Text Books:

1. Mobile Computing – Technology, Applications and Service Creation, Asoke K. Talukder, Roopa R Yavagal, 2nd edition, Tata McGraw Hill, New Delhi, 2009.
2. Mobile Communications, Jochen Schiller, 2nd Edition, Pearson Education, New Delhi, 2008.

Reference Books:

1. The cdma2000 system for Mobile Communications, VieriVanghi, Aleksander Damnjanovic, Pearson Education, New Delhi, 2007.
2. Fundamentals of Mobile and Pervasive Computing, Frank Adelstein, McGraw Hill, New Delhi, 2008.

Online Resources:

1. https://www.tutorialspoint.com/mobile_computing/mobile_computing_overview.htm
2. http://uberthings.com/mobile/#intro
3. http://www.ittoday.info/Articles/Introduction_to_Mobile.htm
4. https://www.cse.wustl.edu/~jain/cse574-16/ftp/j_195g.pdf

L	T	P	C
3	0	0	3

M.Tech. in Digital Electronics and Communication Engineering
I Semester Syllabus
Professional Elective – II
EC116PE: Design of Fault Tolerant Systems

Prerequisites: Digital System Design.

Course Objectives

1. To understand need for testing of manufactured ICs and the testing terminology.
2. To understand the concepts involved in making ICs Fault Tolerant and Self Checking
3. To build digital circuits which are easily testable.

Course Outcomes

After completion of the course the student should be able to

1. Recognize the need for fault models, fault tolerance circuits, controllability, and observability in generation of test vectors for testing digital systems.
2. Explain the principles required to build testable integrated circuits.
3. Demonstrate different approaches to build Fault Tolerant, Self-Checking and Testable Circuits.
4. Analyze the ease with which testing can be performed after applying testing principles in the design of integrated circuits.
5. Estimate the impact of incorporating different DFT architectures into digital designs using RTL code.
6. Design different architectures for Chip Level and System Level DFT.

Course Articulation Matrix

COs	PO1	PO2	PO3	PO4	PO5	PO6
CO1	-	-	2	-	2	-
CO2	2	-	2	3	2	-
CO3	2	-	2	3	2	2
CO4	-	-	3	3	3	-
CO5	2	-	3	3	3	-
CO6	-	-	2	3	2	-

Unit - I

Concepts of Reliability: Reliability, Failures & Faults, Reliability and Failure Rate, Relation between Reliability and Mean Time Between Failure, Maintainability and Availability, Reliability of Series, Parallel and ParallelSeries Combinational Circuits.

Fault Tolerant Design: Basic Concepts, Static, Dynamic, Hybrid, Triple Modular Redundant System (TMR), 5MR Reconfiguration Techniques, Fault Tolerant Design of Memory Systems, Time Redundancy and Software Redundancy.

Unit - II

Self-Checking Circuits & Fail Safe Design: Self Checking Circuits: Basic Concepts of Self Checking Circuits, Design of Totally Self Checking Checker, Checkers for m out of n Codes, Berger Code and Low Cost Residue Code.

Fail Safe Design: Strongly Fault Secure Circuits, Fail Safe Design of Sequential Circuits using Partition Theory and Berger Code, Totally Self Checking PLA Design.

Unit - III

Design for Testability: Need for Testing, Fault Models – Stuck At Faults, Transistor Faults, Bridging Faults, Fault Simulation – Serial, Parallel, Concurrent and Deductive Fault Simulation, Test Generation Basics, Controllability and Observability, SCOAP, Fault – Oriented Test Generation.

Design for Testability by means of scan: Making circuits Testable, Testability Insertion, Full Scan DFT Techniques- Full Scan Insertion, Flip-Flop Structures, Full Scan Design and Test, Scan Architectures–Full Scan Design, Shadow Register DFT, Partial Scan Methods, Multiple Scan Design, Other Scan Designs, RT Level Scan Design – RTL Design Full Scan, RTL Design Multiple Scan, Scan Designs for RTL.

Unit - IV

Logic Built-in-self-test: BIST Basics–Memory Based BIST,BIST Effectiveness, BIST Types, Designing a BIST, Test Pattern Generation - Engaging TPGs, Exhaustive Counters, Ring Counters, Twisted Ring Counter, Linear Feedback Shift Register, Output Response Analysis-Engaging ORA's, One's Counter, Transition Counter, Parity Checking, Serial LFSRs, Parallel Signature Analysis, BIST Architectures-BIST Related Terminologies, Centralized and Separate Board-Level BIST Architecture, Built-in Evaluation and Self Test(BEST), Random Test Socket(RTS), LSSD On-chip Self Test, Self Testing using MISR and SRSG, Concurrent BIST, BILBO, Enhancing Coverage, RT Level BIST Design -CUT Design, Simulation and Synthesis, RTS BIST Insertion, Configuring the RTS BIST, Incorporating Configurations in BIST, Design of STUMPS, RTS and STUMPS Results.

Unit - V

Standard IEEE Test Access Methods: Boundary Scan Basics, Boundary Scan Architecture– Test Access port, Boundary Scan Registers, TAP Controller, Decoder Unit, Select and Other Units, Boundary Scan Test Instructions Mandatory Instructions, Board Level Scan Chain Structure - One Serial Scan Chain, Multiple Scan Chain with One Control Test Port, Multiple Scan Chains with One TDI,TDO but Multiple TMS, Multiple-Scan Chain & Multiple Access Port, RT Level Boundary Scan- Inserting Boundary Scan Test Hardware for CUT, Two Module Test Case, Virtual Boundary Scan Tester, Boundary Scan Description Language.

Text Books:

1. Parag K. Lala, "Fault Tolerant & Fault Testable Hardware Design", PHI, 1985.
2. Zainalabedin Navabi, "Digital System Test and Testable Design using HDL models and Architectures", Springer International Edition, 2014.

Reference Books:

1. Miron Abramovici, Melvin A. Breuer and Arthur D. Friedman, "Digital Systems Testing and Testable Design", JaicoPublishing House, 2006.
2. Bushnell M & Vishwani D. Agarwal, "Essentials of Electronic Testing", Springer, 2004.
3. Laung-Terng Wang, Cheng-Wen Wu, Xiaoqing Wen, "VLSI Test Principles and Architectures: Design for Testability", Morgan Kaufmann, 2006.

Online Resources:

1. https://onlinecourses.nptel.ac.in/noc20_ee76/preview- Digital VLSI Testing by Prof. Santanu Chattopadhyay, Department of Electronics and Electrical Communication Engineering, IIT Kharagpur
2. https://www.youtube.com/watch?v=lRpt1fCHd8Y&list=PLzBynYJnzI5kA05fRGrVlen5WSu12amj3– VLSI Physical Design by Prof Indranil Sengupta, Department of Computer Science and Engineering, IIT Kharagpur

L	T	P	C
2	0	0	2

M.Tech. in Digital Electronics and Communication Engineering
I Semester Syllabus
EC101MC: Research Methodology & Intellectual Property Rights

Course Objectives

The objectives of this course are to make the student

1. To understand the research problem
2. To know the literature studies, plagiarism and ethics
3. To get the knowledge about technical writing
4. To analyze the nature of intellectual property rights and new developments
5. To know the patent rights

Course Outcomes

At the end of this course, students will be able to understand research problem formulation.

1. Analyze research related information Follow research ethics
2. Understand that today's world is controlled by Computer, Information Technology, but tomorrow world will be ruled by ideas, concept, and creativity.
3. Understanding that when IPR would take such important place in growth of individuals & nation, it is needless to emphasis the need of information about Intellectual Property Right to be promoted among students in general & engineering in particular.
4. Understand that IPR protection provides an incentive to inventors for further research work and investment in R & D, which leads to creation of new and better products, and in turn brings about, economic growth and social benefits.

Course Articulation Matrix

COs	PO1	PO2	PO3	PO4	PO5	PO6
CO1	3	3	3	2	3	1
CO2	3	3	2	1	1	1
CO3	-	3	-	1	-	-
CO4	2	2	1	-	1	1

Unit - I

Meaning of research problem, Sources of research problem, Criteria Characteristics of a good research problem, Errors in selecting a research problem, Scope and objectives of research problem. Approaches of investigation of solutions for research problem, data collection, analysis, interpretation, Necessary instrumentations

Unit - II

Effective literature studies approaches, analysis, Plagiarism, Research ethics.

Unit - III

Effective technical writing, how to write report, Paper Developing a Research Proposal, Format of research proposal, a presentation and assessment by a review committee.

Unit - IV

Nature of Intellectual Property: Patents, Designs, Trade and Copyright. Process of Patenting and Development: technological research, innovation, patenting, development. International Scenario: International cooperation on Intellectual Property, Procedure for grants of patents, Patenting under PCT.

Unit - V

Patent Rights: Scope of Patent Rights, Licensing and transfer of technology, Patent information and databases, Geographical Indications, New Developments in IPR: Administration of Patent System, New developments in IPR; IPR of Biological Systems, Computer Software etc. Traditional knowledge Case Studies, IPR and IITs.

Suggested Readings:

1. Stuart Melville and Wayne Goddard, "Research methodology: An Introduction for Science & Engineering Students".
2. Wayne Goddard and Stuart Melville, "Research Methodology: An Introduction".

Reference Books:

1. Ranjit Kumar, "Research Methodology: A Step by Step Guide for beginners", 2nd Edition,
2. Halbert, "Resisting Intellectual Property", Taylor & Francis Ltd, 2007.
3. Mayall, "Industrial Design", McGraw Hill, 1992.
4. Niebel, "Product Design", McGraw Hill, 1974.
5. Asimov, "Introduction to Design", Prentice Hall, 1962.
6. Robert P. Merges, Peter S. Menell, Mark A. Lemley, "Intellectual Property in New Technological Age", 2016.
7. Ramappa .T, "Intellectual Property Rights Under WTO", S. Chand, 2008.

L	T	P	C
2	0	0	0

M.Tech. in Digital Electronics and Communication Engineering
I Semester Syllabus
Audit Course- I
AC101HS: English for Research Paper Writing

Course Outcomes

Students will be able to:

1. Improve their writing skills and level of readability
2. Learn about structure and organization of sections and sub sections
3. Develop requisite skills to write the title
4. Enhance effective writing skills to publish research papers

Unit - I

Planning and Preparation, Word Order, Breaking up long sentences, Structuring Paragraphs and Sentences, Being Concise and Removing Redundancy, Avoiding Ambiguity and Vagueness

Unit - II

Clarifying, Highlighting Findings, Hedging and Criticizing, Paraphrasing and Plagiarism, Sections of a Paper, Abstract, Introduction

Unit - III

Review of the Literature, Methods, Results, Discussion, Conclusions, the Final Check

Unit - IV

Key Skills for: Writing a title, Writing an abstract, Writing an Introduction, Writing a review of the literature

Unit - V

Key skills for: Writing methods, Writing the results, Writing the discussion, Writing the conclusions. Useful phrases and mechanics of effective writing to publish research papers.

Suggested Readings:

1. Adrian Wallwork, English for Writing Research Papers, Springer New York Dordrecht Heidelberg London, 2011.

Reference Books:

1. Goldbort R (2006) Writing for Science, Yale University Press(available on Google Books)
2. Day R (2006) How to Write and Publish a Scientific Paper, Cambridge University Press
3. Highman N (1998), Handbook of Writing for the Mathematical Sciences, SIAM. Highman‟s book.

L	T	P	C
2	0	0	0

M.Tech. in Digital Electronics and Communication Engineering
I Semester Syllabus
Audit Course – I
AC102HS: Disaster Management

Course Objectives

1. Learn to demonstrate a critical understanding of key concepts in disaster risk reduction and humanitarian response.
2. Critically evaluate disaster risk reduction and humanitarian response policy and practice from multiple perspectives.
3. Develop an understanding of standards of humanitarian response and practical relevance in specific types of disasters and conflict situations.
4. Critically understand the strengths and weaknesses of disaster management approaches, planning and programming in different countries, particularly their home country or the countries they work in
5. Provide knowledge about different disasters tools to handle disasters, methods for disaster management

Course Outcomes

1. Understanding disasters, manmade hazards & vulnerabilities
2. Understanding disaster management mechanism
3. Understanding capacity building
4. Understanding concepts
5. Understanding planning of disaster management

Unit - I: Introduction & Disaster Prone Areas in India

Disaster: Definition, Factors and Significance; Difference between Hazard and Disaster; Natural and Manmade Disasters: Difference, Nature, Types and Magnitude. Study of Seismic Zones; Areas prone to Floods and Droughts, Landslides and Avalanches; Areas prone to Cyclonic and Coastal Hazards with special reference to Tsunami; PostDisaster Diseases and Epidemics

Unit - II: Repercussions of Disasters and Hazards

Natural Disasters: Earthquakes, Volcanisms, Cyclones, Tsunamis, Floods, Droughts and Famines, Landslides and Avalanches, Man-made disaster: Nuclear Reactor Meltdown, Industrial Accidents, Oil Slicks and Spills, Outbreaks of Disease and Epidemics, War and Conflicts.

Unit - III: Disaster Preparedness and Management

Preparedness: Monitoring of Phenomena triggering a Disaster or Hazard; Evaluation of Risk: Application of Remote Sensing, Data from Meteorological and other Agencies, Media Reports: Governmental and Community preparedness.

Unit - IV: Risk Assessment

Disaster Risk- Concept and Elements, Disaster Risk Reduction, Global and National Disaster Risk Situation. Techniques of Risk Assessment, Global Co-Operation in Risk Assessment: Risk Assessment and Warning, People‟s Participation in Risk Assessment. Strategies for Survival.

Unit - V: Disaster Mitigation

Meaning, Concept and Strategies of Disaster Mitigation, Emerging Trends in Mitigation. Structural Mitigation and Non-Structural Mitigation, Programs of Disaster Mitigation in India.

Suggested Readings:

1. Nishith R., Singh A K, "Disaster Management in India: Perspectives, issues and strategies ""New Royal book Company.
2. Sahni, Pardeep et. al.," Disaster Mitigation Experiences and Reflections", Prentice Hall of India, New Delhi.
3. Manual on Disaster Management, National Disaster Management, Agency Govt of India.

Reference Books:

1. Goel S.L., Disaster Administration and Management Text and Case Studies", Deep Publication Pvt. Ltd., New Delhi.
2. Pandharinath N., Rajan CK, Earth and Atmospheric Disasters Management BS Publications 2009.
3. National Disaster Management Plan, Ministry of Home affairs, Government of India (http://www.ndma.gov.in/images/policyplan/dmplan/draftndmp.pdf).

L	T	P	C
2	0	0	0

M.Tech. in Digital Electronics and Communication Engineering
I Semester Syllabus
Audit Course – I
AC103HS: Sanskrit for Technical Knowledge

Course Objectives

1. To get a working knowledge in illustrious Sanskrit, the scientific language in the world
2. Learning of Sanskrit to improve brain functioning
3. Learning of Sanskrit to develop the logic in mathematics, science & other subjects enhancing the memory power
4. The engineering scholars equipped with Sanskrit will be able to explore the huge knowledge from ancient literature

Course Outcomes

1. Understanding basic Sanskrit language
2. Ancient Sanskrit literature about science & technology can be understood
3. Being a logical language will help to develop logic in students

Unit - I
Alphabets in Sanskrit

Unit - II
Past / Present / Future Tense, Simple Sentences

Unit - III
Order, Introduction of roots

Unit - IV
Technical information about Sanskrit Literature

Unit - V
Technical Concepts of Engineering - Electrical, Mechanical, Architecture, Mathematics

Suggested Readings:

1. Prathama Deeksha-Vempati Kutumbshastri “Teach Yourself Sanskrit”, Rashtriya Sanskrit Sansthanam, New Delhi Publication

Reference Books:

1. Dr. Vishwas, Samskrita “Abhyaspustakam” -Bharti Publication, New Delhi 2. Suresh Soni “India‟s Glorious Scientific Tradition”, Ocean books (P) Ltd., New Delhi.

L	T	P	C
2	0	0	0

M.Tech. in Digital Electronics and Communication Engineering
I Semester Syllabus
Audit Course – I
AC104HS: Value Education

Course Objectives

1. Understand value of education and self-development
2. Imbibe good values in students
3. Let the should know about the importance of character

Course Outcomes

1. Knowledge of self-development
2. Learn the importance of Human values
3. Developing the overall personality

Unit - I

Values and self-development –Social values and individual attitudes. Work ethics, Indian vision of humanism. Moral and non-moral valuation. Standards and principles. Value judgements

Unit - II

Importance of cultivation of values. Sense of duty. Devotion, Self-reliance. Confidence, Concentration. Truthfulness, Cleanliness. Honesty, Humanity. Power of faith, National Unity. Patriotism. Love for nature, Discipline.

Unit - III

Personality and Behavior Development -Soul and Scientific attitude. Positive Thinking. Integrity and discipline, Punctuality, Love and Kindness.

Unit - IV

Avoid fault Thinking. Free from anger, Dignity of labour. Universal brotherhood and religious tolerance. True friendship. Happiness Vs suffering, love for truth. Aware of self-destructive habits. Association and Cooperation. Doing best for saving nature.

Unit - V

Character and Competence –Holy books vs Blind faith. Self-management and Good health. Science of reincarnation, Equality, Nonviolence, Humility, Role of Women. All religions and same message. Mind your Mind, Self-control. Honesty, Studying effectively.

Suggested Readings:

1. Chakroborty, S.K. “Values and Ethics for organizations Theory and practice”, Oxford University Press, New Delhi.

L	T	P	C
0	0	4	2

M.Tech. in Digital Electronics and Communication Engineering
I Semester Syllabus
EC151PC: Digital System Design Laboratory

Course Objectives

The objectives of this course are to make the student
1. To learn the HDL programming language.
2. To learn the simulation of basic gates using the basic programming language.
3. To learn the simulation of combinational circuits using programming language.
4. To learn the simulation of sequential circuits using programming language.
5. To learn the synthesis and layouts of analog and digital CMOS circuits.
6. To develop an ability to simulate and synthesize various digital circuits.

Course Outcomes

At the end of the course a student will be able to
1. Design of Digital VLSI Circuits, stick diagram of circuits
2. Understand the design Rules of VLSI circuits
3. Understand and simulate speed and power Considerations, Floor Planning and Layout techniques
4. Be able to complete a significant VLSI design project having a set of objective criteria and design constraints.

Course Articulation Matrix

COs	PO1	PO2	PO3	PO4	PO5	PO6
CO1	3	2	2	3	3	2
CO2	2	2	2	3	3	2
CO3	2	2	2	2	3	2
CO4	3	2	3	3	3	2

Part - I

Programming can be done using any complier. Down load the programs on FPGA/CPLD boards and performance testing may be done using pattern generator (32 channels) and logic analyzer apart from verification by simulation with any of the front-end tools.

1. Design and Implement Full Adder, 4-bit Ripple Carry Adder and Carry Look Ahead Adder.
2. Design and Implement 4-bit ALU to Perform – ADD, SUB, AND, OR, XOR, 1's and 2's Complement Operations.
3. Design and Implement 4x1, 8x1 and 16x1 Multiplexer in Dataflow and Structural Model.
4. Design and Implement 1x4, 1x8 and 1x16 Demultiplexer in Dataflow and Structural Model.
5. Design and Implement 2 to 4, 3 to 8 and 4 to16 line decoder in Dataflow and Structural Model.
6. Design and Implement 16-to-4 (With and Without Priority) Encoder in Behavioral Model.
7. Design and Implement Code converters – Binary to BCD code, BCD to Gray code and BCD to Excess -3 code.
8. Design and Implement SR, D, JK, and T flip flops using Behavioral Model.
9. Design and Implement 4-bit Binary and BCD Counters (with Synchronous/ Asynchronous Reset input) using Behavioral Model.

Part - II - Experiments can be done by Mentor Graphics/Cadence/Synapsis/Symica or equivalent tool.

1. Simulate and Verify the Layouts of all CMOS Logic Gates.
2. Simulate and Verify the Layouts of 28 Transistor and 10 Transistor Full Adder.
3. Simulate and Verify the Layout of Full Adder using Dynamic CMOS Technology.
4. Simulate and Verify the Layouts of SR, D, JK And T Flip Flops.
5. Simulate and Verify the Layout of 4-bit Binary Asynchronous/Synchronous Counter

L	T	P	C
0	0	4	2

M.Tech. in Digital Electronics and Communication Engineering
I Semester Syllabus
EC152PC: Wireless Communications and Networks Laboratory

Course Objectives

This course aims to develop
1. Understanding on functioning of wireless communication system and evolution of different wireless communication systems and standards.
2. An ability to compare recent technologies used for wireless communication.
3. An ability to explain the architecture, functioning, protocols, capabilities and application of various wireless communication networks.
4. An ability to explain multiple access techniques for Wireless Communication
5. An ability to evaluate design challenges, constraints and security issues associated with Ad-hoc wireless networks.

Course Outcomes

At the end of this course, students will be able to
1. Implement the advanced digital modulation techniques.
2. Design Convolutional encoder and decoder for error control coding techniques.
3. Calculate path loss for Free space, Okumura and Hata models for outdoor propagation.
4. Comprehend Cellular concepts of GSM and CDMA networks.
5. Simulate RAKE receiver for CDMA with MATLAB.

Course Articulation Matrix

COs	PO1	PO2	PO3	PO4	PO5	PO6
CO1	2	2	3	3	2	2
CO2	2	2	3	3	2	2
CO3	1	2	2	2	2	2
CO4	1	2	2	2	1	1
CO5	2	2	2	3	2	2

List of Experiments:

1. FSK Modulation and Demodulation technique.
2. QPSK Modulation and Demodulation technique.
3. DQPSK Modulation and Demodulation technique
4. 8-QAM Modulation and Demodulation technique.
5. Implementation of Convolutional Encoder and Decoder.
6. Simulation of the following Outdoor Path loss propagation models using MATLAB.
   a. Free Space Propagation model b. Okumura model c. Hata model
7. Simulation of Adaptive Linear Equalizer using MATLAB software.
8. Measurement of call blocking probability for GSM &CDMA networks using Netsim software.
9. Study of GSM handset for various signaling and fault insertion techniques (Major GSM handset sections: clock, SIM card, charging, LCD module, Keyboard, User interface).
10. Study of transmitter and receiver section in mobile handset and measure frequency band signal and GMSK modulating signal.

11. Simulation of RAKE Receiver for CDMA communication using MATLAB software.
12. Simulate and test various types of PN codes, chip rate, spreading factor and processing gain on performance of DSSS in CDMA.
13. Simulate and test the 3G Network system features using GSM AT Commands. (Features of 3G Communication system: Transmission of voice, video calls, SMS, MMS, TCP/IP, HTTP, GPS)
14. Modeling of communication system using Simulink.

Note: Experiments 1 to 5 need to be simulated using MATLAB and tested on hardware**.**

L	T	P	C
3	0	0	3

M.Tech. in Digital Electronics and Communication Engineering
II Semester Syllabus
EC201PC: ARM Microcontrollers and Programmable Digital Signal Processors

Course Objectives

Students undergoing this course are expected to
1. To understand the internal architecture of ARM Cortex M3.
2. To provide basics of Exceptions and Interrupts.
3. To impart knowledge of Programmable DSP (P-DSP) Processors.
4. To familiarize the internal architecture of TMS320C6000 series

Course Outcomes

1. Narrate the basic features of the Cortex-M3 processor, applications, list its instruction set, and outline the memory attributes.
2. Classify and illustrate exceptions and interrupts for interfacing peripherals with CortexM3 and characterize the NVIC.
3. Identify the architectural features of P-DSP processors, and apply the MAC unit and barrel shifter for real-time computations.
4. Distinguish between the TI DSP processor family, Cortex-M3 versions, and compare their instruction sets, memory configurations, and related software development tools.
5. Interpret the VLIW architectural features, addressing modes, instruction sets, and on-chip peripherals of TMC320C6000 series processors and develop application programs using the code composer studio tool.

Course Articulation Matrix

COs	PO1	PO2	PO3	PO4	PO5	PO6
CO1	-	-	3	2	3	1
CO2	-	-	2	2	3	1
CO3	1	-	2	3	3	1
CO4		-	2	3	3	1
CO5	2	-	2	3	3	1

Unit - I

ARM Cortex-M3 processor: Applications, Programming model – Registers, Operation modes, Exceptions and Interrupts, Reset Sequence Instruction Set, Unified Assembler Language, Memory Maps, Memory Access Attributes, Permissions, Bit-Band Operations, Unaligned and Exclusive Transfers. Pipeline, Bus Interfaces.

Unit - II

Exceptions: Exceptions, Types, Priority, Vector Tables, Interrupt Inputs and Pending behavior, Fault Exceptions, Supervisor and Pendable Service Call.

Unit - III

Interrupts: Nested Vectored Interrupt Controller, Basic Configuration, SYSTICK Timer, Interrupt Sequences, Exits, Tail Chaining, Interrupt Latency.

Unit - IV

Programmable DSP (P-DSP) Processors: Harvard Architecture, Multi-port memory, Architectural structure of P-DSP- MAC unit, Barrel shifters, Introduction to TI DSP processor family.

Unit - V

VLIW architecture and TMS320C6000 series: Architecture study, Data paths, Cross paths, Introduction to Instruction level architecture of C6000 family, Assembly Instructions memory addressing, for arithmetic, logical operations. Code Composer Studio for application development for Digital signal processing, on chip peripherals, Processor benchmarking.

Suggested Readings:

1. Joseph Yiu, "The definitive guide to ARM Cortex-M3", Elsevier, 2nd Edition, 2011.
2. Venkatramani B. and Bhaskar M. "Digital Signal Processors: Architecture, Programming and Applications", TMH, 2nd Edition, 2002.
3. Sloss Andrew N, Symes Dominic, Wright Chris, "ARM System Developer's Guide: Designing and Optimizing", Morgan Kaufman Publication 2nd Edition, 2004.

Reference Books:

1. Steve Furber, "ARM System-on-Chip Architecture", Pearson Education, 2nd Edition, 2001.
2. Frank Vahid, Tony Givargis, "Embedded System Design a Unified Hardware Software Introduction", John Wiley India, Edition-Student edition, 2014.

L	T	P	C
3	0	0	3

M.Tech. in Digital Electronics and Communication Engineering
II Semester Syllabus
EC202PC: Advanced Communications and Networks

Course Objectives

The objectives of this course are to make the student
1. To acquire the knowledge in Orthogonal Frequency Division Multiplexing and Spread Spectrum Communications.
2. To study the MIMO Systems.
3. To study the various Wireless LANs and PANs.

Course Outcomes

At the end of this course, students will be able to
1. Understand the concepts of Orthogonal Frequency Division Multiplexing and Spread Spectrum Communications.
2. Understand the concepts MIMO Systems
3. Acquire the knowledge of different Wireless LANs and PANs

Course Articulation Matrix

COs	PO1	PO2	PO3	PO4	PO5	PO6
CO1	2	-	2	1	3	2
CO2	2	-	2	3	3	2
CO3	2	-	2	1	3	2

Unit - I

Spread Spectrum Communications: Spreading sequences- Properties of Spreading Sequences, Pseudo- noise sequence, Gold sequences, Kasami sequences, Walsh Sequences, Orthogonal Variable Spreading Factor Sequences, Barker Sequence, Complementary Codes Direct sequence spread spectrum: DS-CDMA Model, Conventional receiver, Rake Receiver, Synchronization in CDMA, Power Control, Soft handoff, Multiuser detection – Optimum multiuser detector, Liner multiuser detection.

Unit - II

Orthogonal Frequency Division Multiplexing: Basic Principles of Orthogonality, Single vs Multicarrier Systems, OFDM Block Diagram and Its Explanation, OFDM Signal Mathematical Representation, Selection parameter for Modulation, Pulse shaping in OFDM Signal and Spectral Efficiency, Window in OFDM Signal and Spectrum, Synchronization in OFDM, Pilot Insert in OFDM Transmission and Channel Estimation, Amplitude Limitations in OFDM, FFT Point Selection Constraints in OFDM, CDMA vs OFDM, Hybrid OFDM.

Unit - III

MIMO Systems: Introduction, Space Diversity and System Based on Space Diversity, Smart Antenna system and MIMO, MIMO Based System Architecture, MIMO Exploits Multipath, Space – Time Processing, Antenna Consideration for MIMO, MIMO Channel Modelling, MIMO Channel Measurement, MIMO Channel. Capacity, Cyclic Delay Diversity (CDD), Space Time Coding, Advantages and Applications of MIMO in Present Context, MIMO Applications in 3G Wireless System and Beyond, MIMO-OFDM.

Unit - IV

Wireless LANs/IEEE 802.11x: Introduction to IEEE802.11x Technologies, Evolution of wireless LANs, IEEE 802.11 Design Issues, IEEE 802.11 Services, IEEE 802.11 MAC Layer operations, IEEE 802.11 Layer1, IEEE 802.11 a/b/g Higher Rate Standards, Wireless LAN Security, Computing Wireless Technologies, Typical WLAN Hardware.

Unit - V

Wireless PANs/IEEE 802.15x: Introduction to IEEE 802.15x Technologies: Wireless PAN Applications and Architecture, IEEE 802.15.1 Physical Layer Details, Bluetooth Link Controllers Basics, Bluetooth Link Controllers Operational States, IEEE 802.15.1 Protocols and Host Control Interface. Evaluation of IEEE 802.15 Standards

Broad Band Wireless MANs/IEEE 802.16x: Introduction to WMAN/IEEE 802.16x Technology, IEEE 802.16 Wireless MANs, IEEE 802.16 MAC Layer Details, IEEE 802.16 Physical Layer Details, IEEE 802.16 Physical Layer Details for 2-11 GHz, IEEE 802.16 Common System Operations.

Suggested Readings:

1. Gary J. Mullett, “Introduction to Wireless Telecommunications Systems and Networks”, CENGAGE. 2. Upena Dalal, “Wireless Communication”, Oxford University Press, 2009

Reference Books:

1. Ke-Lin Du & M N S Swamy, “Wireless Communication System”, Cambridge University Press, 2010. 2. Gottapu Sasibhusan Rao, “Mobile Cellular Communication”, PEARSON

L	T	P	C
3	0	0	3

M.Tech. in Digital Electronics and Communication Engineering
II Semester Syllabus
Professional Elective-III
EC211PE: Embedded Systems Design

Course Objectives

The objectives of this course are to make the student
1. To provide an overview of Design Principles of Embedded System.
2. To provide clear understanding about the role of firmware, operating systems in correlation with hardware systems.

Course Outcomes

At the end of this course, students will be able to
1. Expected to understand the selection procedure of Processors in the Embedded domain.
2. Design Procedure for Embedded Firmware.
3. Expected to visualize the role of Real time Operating Systems in Embedded Systems
4. Expected to evaluate the Correlation between task synchronization and latency issues

Course Articulation Matrix

COs	PO1	PO2	PO3	PO4	PO5	PO6
CO1	-	-	2	3	2	-
CO2	2	-	2	3	3	-
CO3	-	-	2	2	2	-
CO4	-	-	-	3	2	2

Unit - I

Introduction to Embedded Systems: Definition of Embedded System, Embedded Systems Vs General Computing Systems, History of Embedded Systems, Classification, Major Application Areas, Purpose of Embedded Systems, Characteristics and Quality Attributes of Embedded Systems.

Unit - II

Typical Embedded System: Core of the Embedded System: General Purpose and Domain Specific Processors, ASICs, PLDs, Commercial Off-The-Shelf Components (COTS), Memory: ROM, RAM, Memory according to the type of Interface, Memory Shadowing, Memory selection for Embedded Systems, Sensors and Actuators- Light Dependent Resistor, Thermistor, Photo Transistor, Light Emitting Diode, Relays, Stepper Motor. Communication Interfaces: SPI, I2C, UART, Onboard and External Communication Interfaces: WiFi, Bluetooth, ZigBee, USB

Unit - III

Other System Components of Embedded system: Reset Circuit, Brown-out Protection Circuit, Oscillator Unit, Real Time Clock, Watchdog Timer, Embedded Firmware Design Approaches: Super Loop Based Approach and OS based Approach, Development Languages: Assembly Language and High level Language

Unit - IV

RTOS Based Embedded System Design: Operating System Basics, Types of Operating Systems-GPOS, RTOS, Tasks, Task States, Task Control Block, Process and Threads, Multiprocessing and Multitasking, Task Scheduling Non-Preemptive Scheduling (FCFS, LCFS, SJF, Priority Based), Preemptive Scheduling(FCFS, LCFS, SJF, Priority Based, Round-Robin).

Unit - V

Task Communication: Shared Memory, Message Passing, Remote Procedure Call and Sockets, Task Communication/Synchronization Issues: Racing, Deadlock, Live lock, Starvation, Task Synchronization Techniques: Mutual exclusion through busy waiting/ Spin lock, Mutual exclusion through Sleep and Wakeup, Semaphores, Device Drivers, Methods to Choose an RTOS.

Suggested Readings:

1. Shibu K.V, Introduction to Embedded Systems, Mc Graw Hill.

Reference Books:

1. Raj Kamal, Embedded Systems, TMH.
2. Frank Vahid, Tony Givargis Embedded Systems Design: A Unified Hardware/Software Introduction, John & Wiley Publications, 2002.
3. Lyla B. Das, Embedded Systems, Pearson, 2013.
4. David E. Simon, An Embedded Software Primer, Pearson Education.

L	T	P	C
3	0	0	3

M.Tech. in Digital Electronics and Communication Engineering
II Semester Syllabus
Professional Elective-III
EC212PE: Low Power CMOS VLSI Design

Prerequisites: CMOS VLSI Design

Course Objectives

1. To Develop CMOS Digital Circuits for a Low Voltage Low Power Environment.
2. To Acquire the Knowledge on the Concepts of Device Behavior and Modelling.
3. To Understand the Concepts of Low Voltage, Low Power Circuits.
4. To Design Low Power Memory and Microprocessor Systems.

Course Outcomes

After completion of the course the student should be able to

1. Describe the concept of low power design and physics of power.
2. Realize the impact of power on system performance and reliability
3. Develop Knowledge about different Low power estimation Techniques.
4. Familiarize on various leakage sources and reduction techniques.
5. Estimate power dissipation in clock distribution
6. Design and develop low power Memory and Microprocessor systems.

Course Articulation Matrix

COs	PO1	PO2	PO3	PO4	PO5	PO6
CO1	-	-	2	2	2	-
CO2	-	-	2	2	2	2
CO3	2	-	2	3	2	-
CO4	-	-	2	3	2	-
CO5	-	-	2	-	3	-
CO6	2	-	2	3	3	-

Unit - I

Technology & Circuit Design Levels: Sources of power dissipation in digital ICs, degree of freedom, recurring themes in low-power, emerging low power approaches, dynamic dissipation in CMOS, effects of Vdd and Threshold voltage on speed, constraints on Threshold voltage reduction, transistor sizing & optimal gate oxide thickness, impact of technology scaling, technology innovations.

Unit - II

Low Power Circuit Techniques: Power consumption in circuits, flip-flops &latches, high capacitance nodes, energy recovery, reversible pipelines, high performance approaches.

Unit - III

Low Power Clock Distribution: Power dissipation in clock distribution, single driver versus distributed buffers, buffers & device sizing under process variations, zero skew Vs tolerable skew, chip & package co-design of clock network.

Unit - IV

Logic Synthesis for Low Power estimation techniques: Power minimization techniques, Low power arithmetic components- circuit design styles, adders, multipliers.

Low Power Memory Design: Sources & reduction of power dissipation in memory Subsystem, sources of power dissipation in DRAM & SRAM, low power DRAM circuits, low power SRAM circuits.

Unit - V

Low Power Microprocessor Design System: Power management support, architectural trade offs for power, choosing the supply voltage, low-power clocking, implementation problem for low power, comparison of microprocessors for power &performance.

Text Books :

1. Rabaey, Jan M., Pedram, Massoud, "Low Power Design Methodologies" Springer US Publisher, 1996.
2. Kaushik Roy, Sharat Prasad, "Low power CMOS VLSI circuit design", John Wiley sons Inc., 2000.

Reference Books:

1. P. Rashinkar, Paterson and L. Singh, "Low Power Design Methodologies", Kluwer Academic, 2002
2. J.B.Kulo and J.H Lou, "Low voltage CMOS VLSI Circuits", Wiley, 1999.
3. A.P.Chandrasekaran and R.W.Broadersen, "Low power digital CMOS design", Kluwer, 1995.
4. Gary Yeap, "Practical low power digital VLSI design", Kluwer, 1998.

Online Resources

1. https://nptel.ac.in/courses/106105034 (Course Title: Low Power VLSI Circuits and Systems by Prof. Ajit Paul, IIT Kharagpur)
2. https://freevideolectures.com/course/4717/nptel-vlsi-physical-design/58 (Course Title: VLSI Physical Design by Prof.Indranil Sengupta, IIT Kharagpur)

L	T	P	C
3	0	0	3

M.Tech. in Digital Electronics and Communication Engineering
II Semester Syllabus
Professional Elective-III
CS213PE: Computer Vision

Prerequisites: Digital Signal Processing

Course Objectives

1. Familiarize the students with the theoretical aspects of computing with images.
2. Understand the concepts of image filtering, edge detection, Feature extraction, Edges, Texture and shape representation.
3. Applying basic mathematical morphology concepts and segmentation.
4. Identifying different patterns using various pattern analysis techniques.

Course Outcomes

After completion of the course the student should be able to

1. Define the fundamental concepts of image processing and Computer Vision.
2. Identify the various operations and methods in field of Computer Vision.
3. Get familiar with methods and apply in computer vision-filtering, edge detection, texture representation, morphological processing and segmentation.
4. Distinguish between the various operations of image analysis.
5. Formulate a computer vision application and perform the operations of pattern analysis.
6. Design and validated the computational approach to computer vision problems and interpret the results to assess the performance.

Course Articulation Matrix

COs	PO1	PO2	PO3	PO4	PO5	PO6
CO1	-	-	2	3	2	-
CO2	2	-	3	2	2	-
CO3	2	-	3	3	2	-
CO4	2	-	3	3	2	2
CO5	2	-	3	2	3	-
CO6	2	-	3	3	3	2

Unit - I

Image Processing: Fundamental steps in Digital image processing, Components of an Image Processing System, Image sensing and acquisition, Image sampling and quantization, Basic relationships between pixels. **LINEAR FILTERS:**, Introduction to Computer Vision ,Linear Filters and Convolution, Shift Invariant Linear Systems, Spatial Frequency and Fourier Transforms, A Continuous Model of a Sampled Signal, Aliasing, Filters as Templates, Technique: Normalized Correlation and Finding Patterns, Technique: Scale and Image Pyramids.

Unit – II

Edge Detection: Noise- Additive Stationary Gaussian Noise, Why Finite Differences Respond to Noise, Estimating Derivatives - Derivative of Gaussian Filters, Why Smoothing Helps, Choosing a Smoothing Filter, Why Smooth with a Gaussian? Detecting Edges-Using the Laplacian to Detect Edges, Gradient-Based Edge Detectors, Technique: Orientation Representations and Corners.

Unit - III

Feature Extraction: Histogram Processing, Color: Color Fundamentals, Color Models, Texture: Representing Texture - Extracting Image Structure with Filter Banks, Representing Texture Using the Statistics of Filter Outputs, Analysis (and Synthesis) Using Oriented Pyramids –The Laplacian Pyramid, Filters in the Spatial Frequency Domain, Oriented Pyramids, Application: Synthesizing Textures for Rendering, Homogeneity, Synthesis by Sampling Local Models, Shape from Texture, Shape from Texture for Planes, Shape from Texture for Curved Surfaces.

Unit – IV

Mathematical Morphology: Erosion and Dilation, Opening and Closing.

Segmentation By Clustering: What is Segmentation, Human Vision: Grouping and Gestalt, Applications: Shot Boundary Detection and Background Subtraction, Image Segmentation by Clustering Pixels, Segmentation by Graph Theoretic Clustering. The Hough Transform, Fitting Lines, Fitting Curves. The Use of Motion in Segmentation.

Unit - V

Pattern Analysis: Clustering: K-Means, K-Medoids, Mixture of Gaussians, Classification: Supervised, Un-supervised, Semi supervised, Classifiers: Bayesian Statistics, KNN, Dimensionality Reduction: PCA, ICA.

Text Books:

1. R C Gonzalez &R E woods, Digital Image Processing, Addison Pearson, 3ed.
2. David A.Forsyth, Jean Ponce, Computer Vision-A Modern Approach, PHI, 2003.
3. Goodfellow, Y Bengio, A Courville, Deep Learning, MIT Press, 2016

Reference Books:

1. Richard Szeliski Computer Vision: Algorithms and Applications, Springer; 2011th edition.
2. Robert B. Fisher, Toby P. Breckon, Kenneth Dawson-Howe, Andrew Fitzgibbon, Craig Robertson, Emanuele Trucco, Christopher K. I. Williams, Dictionary of Computer Vision and Image Processing, Wiley, 2013.

Online Resources:

1. https://nptel.ac.in/courses/106105216 (Course Title: Computer Vision, IIT Kharagpur, Prof. Jayanta Mukhopadhyay).
2. http://groups.csail.mit.edu/vision/courses/6.869/materials.html.
3. http://www.cl.cam.ac.uk/teaching/1516/CompVision/materials.html.

L	T	P	C
3	0	0	3

M.Tech. in Digital Electronics and Communication Engineering
II Semester Syllabus
Professional Elective-IV
EC214PE: Deep Learning

Prerequisites: Digital Signal Processing

Course Objectives

1. Introduce to the basic concepts of neural networks.
2. Identify and analyze the various types of neural networks and models of neuron and apply accordingly.
3. Introduce the concept of deep learning and its types.
4. Explore the concepts of applications of deep learning.

Course Outcomes

Upon completing this course students will be able to:

1. Analyze and apply the basic the concepts of neural networks
2. Analyze various types of neural networks and use various activation functions to solve complex problems.
3. Relate the concept of deep learning and its architecture.
4. Design and carry out empirical analysis for various types of applications of deep learning systems.

Course Articulation Matrix

COs	PO1	PO2	PO3	PO4	PO5	PO6
CO1	3	-	2	3	3	2
CO2	-	-	2	2	3	2
CO3	-	-	3	2	2	-
CO4	3	-	2	3	2	2

Unit - I

Introduction to Neural networks: Characteristics of Neural Networks, Historical Development of Neural Networks Principles, Artificial Neural Networks: Terminology, Models of Neuron, Topology, Basic Learning Laws, Pattern Recognition Problem, Basic Functional Units, Pattern Recognition Tasks by the Functional Units: Introduction, Analysis of pattern Association Networks, Analysis of Pattern Classification Networks, Analysis of pattern storage Networks, Analysis of Pattern Mapping Networks.

Unit - II

Feedback Neural Networks: Introduction, Analysis of Linear Auto associative FF Networks, Analysis of Pattern Storage Networks, Competitive Learning Neural Networks & Complex pattern Recognition Introduction, Analysis of Pattern Clustering Networks, Analysis of Feature Mapping Networks, Associative Memory.

Unit - III

Fundamentals of Deep Learning: Defining Deep Learning, Common architectural principles of Deep Networks, Building Blocks of Deep Networks, and Major architectures of Deep Networks: Unsupervised Pretrained Networks, Convolution Neural Networks (CNNs), Recurrent Neural Networks.

Unit - IV

Convolution Neural Networks: The convolution operation, motivation, pooling, Convolution and Pooling as an Infinitely Strong Prior, Applications of deep learning: Large scale deep learning, Computer vision, Speech Recognition, Natural Processing, other applications.

Unit - V

Sequential Modelling: Recurrent neural networks: Recursive neural networks, The long short–term Memory, explicit memory, Auto encoders: Under complete, regularized, Stochastic Encoders and Decoders, Denoising Auto encoders.

Suggested Readings:

1. Yagna Narayana. B, Artificial Neural Networks, PHI.(Chapter 1,2 and 3)
2. Patterson Josh, Gibson Adam, Deep Learning: A Practitioner's Approach.
3. Bengio, Yoshua, Ian J. Goodfellow, and Aaron Courville. "Deep learning." An MIT Press book in preparation. (2015)-http://www.deeplearningbook.org/

Reference Books:

1. Simon Haykin, Neural Networks, PHI
2. Ian Good Fellow, Yoshua Bengio, Aran Courville, Deep learning (Adaptive computation & Machine learning).
3. Fausett**,** Fundamentals of Neural Networks: Architectures, Algorithms and Applications.

L	T	P	C
3	0	0	3

M.Tech. in Digital Electronics and Communication Engineering
II Semester Syllabus
Professional Elective – IV
EC215PE: Pattern Recognition and Machine Learning

Course Objectives

The student will be able to understand the mathematical formulation of patterns.
1. To study the various linear models.
2. Understand the basic classifiers.
3. Can able to distinguish different models.

Course Outcomes

On completion of this course student will be able to
1. Learn the basics of pattern classes and functionality.
2. Construct the various linear models.
3. Understand the importance kernel methods.
4. Learn the Markov and Mixed models

Course Articulation Matrix

COs	PO1	PO2	PO3	PO4	PO5	PO6
CO1	-	-	3	2	3	2
CO2	2	-	3	3	3	-
CO3	-	-	3	2	3	2
CO4	-	-	2	3	2	1

Unit - I

Introduction to Pattern recognition: Mathematical Formulation and Basic Functional Equation, Reduction of Dimensionality, Experiments in Pattern Classification, Backward Procedure for Both Feature Ordering- and Pattern Classification, Suboptimal Sequential Pattern Recognition, Nonparametric Design of Sequential Pattern Classifiers, Analysis of Optimal Performance and a Multiclass Generalization

Unit - II

Linear Models: Linear Basis Function Models -Maximum likelihood and least squares, Geometry of least squares , Sequential learning, Regularized least squares, Multiple outputs , The Bias-Variance Decomposition, Bayesian Linear Regression -Parameter distribution, Predictive, Equivalent, Bayesian Model Comparison, Probabilistic Generative Models-Continuous inputs , Maximum likelihood solution, Discrete features, Exponential family, Probabilistic Discriminative Models -Fixed basis functions, Logistic regression, Iterative reweighted least squares, Multiclass logistic regression, Probit regression, Canonical link functions

Unit - III

Kernel Methods: Constructing Kernels, Radial Basis Function Networks - Nadaraya-Watson model, Gaussian Processes -Linear regression revisited, Gaussian processes for regression, Learning the hyper parameters, Automatic relevance determination, Gaussian processes for classification, Laplace approximation, Connection to neural networks, Sparse Kernel Machines- Maximum Margin Classifiers, Overlapping class distributions, Relation to logistic regression, Multiclass SVMs, SVMs for regression, Computational learning theory, Relevance Vector Machines- RVM for regression, Analysis of sparsity, RVM for classification.

Unit - IV

Graphical Models: Bayesian Networks, Example: Polynomial regression, Generative models, Discrete variables, Linear-Gaussian models, Conditional Independence- Three example graphs, D- separation, Markov Random Fields -Conditional independence properties, Factorization properties, Illustration: Image de-noising, Relation to directed graphs, Inference in Graphical Models- Inference on a chain, Trees, Factor graphs, The sum-product algorithm, The max-sum algorithm, Exact inference in general graphs, Loopy belief propagation, Learning the graph structure.

Unit - V

Mixture Models and EM algorithm: K-means Clustering-Image segmentation and compression, Mixtures of Gaussians-Maximum likelihood, EM for Gaussian mixtures, An Alternative View of EM- Gaussian mixtures revisited, Relation to K-means, Mixtures of Bernoulli distributions, EM for Bayesian linear regression, The EM Algorithm in General, Combining Models- Tree-based Models, Conditional Mixture Models- Mixtures of linear regression models, Mixtures of logistic models, Mixtures of experts.

Suggested Readings:

1. K. S. Fu, Sequential methods in Pattern Recognition and Machine Learning, Academic Press, volume no.52.
2. Pattern Recognition and Machine Learning- C. Bishop-Springer, 2006.

Reference Books:

1. Richard o. Duda, Peter E. hart, David G. Stork, Pattern Classification, John Wiley& Sons, 2nd Ed., 2001.
2. Trevor Hastie, Robert Tibshirani, Jerome H. Friedman, The elements of Statistical Learning, Springer, 2nd Ed., 2009.

L	T	P	C
3	0	0	3

M.Tech. in Digital Electronics and Communication Engineering
II Semester Syllabus
Professional Elective – IV
EC216PE: Ad-hoc and Wireless Sensor Networks

Course Objectives

The objectives of this course are to make the student
1. To study the fundamentals of wireless Ad-Hoc Networks.
2. To study the operation and performance of various ad-hoc wireless network protocols.
3. To study the architecture and protocols of Wireless sensor networks

Course Outcomes

On completion of this course student will be able to
1. Students will be able to understand the basis of Ad-hoc wireless networks.
2. Students will be able to understand design, operation and the performance of MAC layer protocols of adhoc wireless networks.
3. Students will be able to understand design, operation and the performance of routing protocol of ad-hoc wireless network.
4. Students will be able to understand design, operation and the performance of transport layer protocol of adhoc wireless networks.
5. Students will be able to understand sensor network Architecture and will be able to distinguish between protocols used in ad-hoc wireless network and wireless sensor networks.

Course Articulation Matrix

COs	PO1	PO2	PO3	PO4	PO5	PO6
CO1	-	-	2	2	2	-
CO2	2	-	2	3	2	-
CO3	2	-	2	3	2	-
CO4	2	-	2	3	3	-
CO5	-	-	2	3	2	-

Unit - I

Wireless LANs and PANs: Introduction, Fundamentals of WLANS, IEEE 802.11 Standards, HIPERLAN Standard, Bluetooth, Home RF.

AD HOC WIRELESS NETWORKS: Introduction, Issues in Ad Hoc Wireless Networks.

Unit - II

MAC Protocols: Introduction, Issues in Designing a MAC protocol for Ad Hoc Wireless Networks, Design goals of a MAC Protocol for Ad Hoc Wireless Networks, Classifications of MAC Protocols, Contention - Based Protocols, Contention - Based Protocols with reservation Mechanisms, Contention – Based MAC Protocols with Scheduling Mechanisms, MAC Protocols that use Directional Antennas, Other MAC Protocols.

Unit - III

Routing Protocols: Introduction, Issues in Designing a Routing Protocol for Ad Hoc Wireless Networks, Classification of Routing Protocols, Table –Driven Routing Protocols, On – Demand Routing Protocols, Hybrid Routing Protocols, Routing Protocols with Efficient Flooding Mechanisms, Hierarchical Routing Protocols, Power – Aware Routing Protocols.

Unit - IV

Transport Layer Protocols: Introduction, Issues in Designing a Transport Layer Protocol for Ad Hoc Wireless Networks, Design Goals of a Transport Layer Protocol for Ad Hoc Wireless Networks, Classification of Transport Layer Solutions, TCP Over Ad Hoc Wireless Networks, Other Transport Layer Protocol for Ad Hoc Wireless Networks.

Unit - V

Wireless Sensor Networks: Introduction, Sensor Network Architecture, Data Dissemination, Data Gathering, MAC Protocols for Sensor Networks, Location Discovery, Quality of a Sensor Network, Evolving Standards, Other Issues.

Suggested Readings:

1. Siva Ram Murthy. C and Manoj B. S, Ad Hoc Wireless Networks: Architectures and Protocols, PHI, 2004.
2. Jagannathan Sarangapani, Wireless Ad- hoc and Sensor Networks: Protocols, Performance and Control, CRC Press.

Reference Books:

1. Toh C. K, Ad-Hoc Mobile Wireless Networks: Protocols & Systems, 1st Ed. Pearson Education.
Raghavendra C. S and Krishna M. Sivalingam, Wireless Sensor Networks, Springer, 2004.

L	T	P	C
2	0	0	0

M.Tech. in Digital Electronics and Communication Engineering
II Semester Syllabus
Audit Course - II
AC201HS: Constitution of India

Course Objectives

The objectives of this course are to make the student

1. Understand the premises informing the twin themes of liberty and freedom from a civil rights perspective.
2. To address the growth of Indian opinion regarding modern Indian intellectuals‟ constitutional role and entitlement to civil and economic rights as well as the emergence of nationhood in the early years of Indian nationalism.
3. To address the role of socialism in India after the commencement of the Bolshevik Revolution in 1917 and its impact on the initial drafting of the Indian Constitution

Course Outcomes

On completion of this course student will be able to

1. Discuss the growth of the demand for civil rights in India for the bulk of Indians before the arrival of Gandhi in Indian politics.
2. Discuss the intellectual origins of the framework of argument that informed the conceptualization of social reforms leading to revolution in India.
3. Discuss the circumstances surrounding the foundation of the Congress Socialist Party [CSP] under the leadership of Jawaharlal Nehru and the eventual failure of the proposal of direct elections through adult suffrage in the Indian Constitution.
4. Discuss the passage of the Hindu Code Bill of 1956.

Unit - I

History of Making of the Indian Constitution: History Drafting Committee, (Composition & Working),
Philosophy of the Indian Constitution: Preamble**,** Salient Features.

Unit - II

Contours of Constitutional Rights & Duties: Fundamental Rights Right to Equality**,** Right to Freedom**,** Right against Exploitation**,** Right to Freedom of Religion**,** Cultural and Educational Rights**,** Right to Constitutional Remedies, Directive Principles of State Policy**,** Fundamental Duties.

Unit - III

Organs of Governance: Parliament**,** Composition**,** Qualifications and Disqualifications**,** Powers and Functions**,** Executive**,** President**,** Governor**,** Council of Ministers, Judiciary, Appointment and Transfer of Judges, Qualification, Powers and Functions.

Unit - IV

Local Administration: District's Administration head: Role and Importance, Municipalities: Introduction, Mayor and role of Elected Representative, CEO of Municipal Corporation. Pachayati raj: Introduction, PRI: Zila Pachayat. Elected officials and their roles, CEO Zila Pachayat: Position and role. Block level: Organizational Hierarchy (Different departments), Village level: Role of Elected and Appointed officials, Importance of grass root democracy.

Unit - V

Election Commission: Election Commission: Role and Functioning. Chief Election Commissioner and Election Commissioners. State Election Commission: Role and Functioning. Institute and Bodies for the welfare of SC/ST/OBC and women.

Suggested Readings/ References:

1. The Constitution of India, 1950 (Bare Act), Government Publication.
2. Dr. S. N. Busi, Dr. B. R. Ambedkar framing of Indian Constitution, 1st Edition, 2015.
3. M. P. Jain, Indian Constitution Law, 7th Edn., Lexis Nexis, 2014.
4. D.D. Basu, Introduction to the Constitution of India, Lexis Nexis, 2015.

L	T	P	C
2	0	0	0

M.Tech. in Digital Electronics and Communication Engineering
II Semester Syllabus
Audit Course - II
AC202HS: Pedagogy Studies

Course Objectives

1. Review existing evidence on the review topic to inform programme design and policy making undertaken by the DFID, other agencies and researchers.
2. Identify critical evidence gaps to guide the development.

Course Outcomes

1. What pedagogical practices are being used by teachers in formal and informal classrooms in developing countries?
2. What is the evidence on the effectiveness of these pedagogical practices, in what conditions, and with what population of learners?
3. How can teacher education (curriculum and practicum) and the school curriculum and guidance materials best support effective pedagogy?

Unit - I

Introduction and Methodology: Aims and rationale, Policy background, Conceptual framework and terminology, Theories of learning, Curriculum, Teacher education. Conceptual framework, Research questions. Overview of methodology and Searching.

Unit - II

Thematic overview: Pedagogical practices are being used by teachers in formal and informal classrooms in developing countries. Curriculum, Teacher education.

Unit - III

Evidence on the effectiveness of pedagogical practices, Methodology for the indepth stage: quality assessment of included studies. How can teacher education (curriculum and practicum) and the scho curriculum and guidance materials best support effective pedagogy? Theory of change. Strength and nature of the body of evidence for effective pedagogical practices. Pedagogic theory and pedagogical approaches. Teachers‟ attitudes and beliefs and Pedagogic strategies.

Unit - IV

Professional development: alignment with classroom practices and follow-up support, Peer support, Support from the head teacher and the community. Curriculum and assessment, Barriers to learning: limited resources and large class sizes.

Unit - V

Research gaps and future directions: Research design, Contexts, Pedagogy, Teacher education, Curriculum and assessment, Dissemination and research impact.

Suggested Readings:

1. Ackers J, Hardman F (2001) Classroom interaction in Kenyan primary schools, Compare, 31 (2): 245-261.
2. Agrawal M (2004) Curricular reform in schools: The importance of evaluation, Journal of Curriculum Studies, 36 (3): 361-379.
3. Alexander RJ (2001) Culture and pedagogy: International comparisons in primary education. Oxford and Boston: Blackwell. 4. Chavan M (2003) Read India: A mass scale, rapid, „learning to read‟ campaign.

Reference Books:

1. Akyeampong K (2003) Teacher training in Ghana -does it count? Multi-site teacher education research project (MUSTER) country report 1. London: DFID.
2. Akyeampong K, Lussier K, Pryor J, WestbrookJ (2013) Improving teaching and learning of basic maths and reading in Africa: Does teacher preparation count? International Journal Educational Development, 33 (3): 272–282.
3. www.pratham.org/images/resource%20working%20paper%202.pdf.

L	T	P	C
2	0	0	0

M.Tech. in Digital Electronics and Communication Engineering
II Semester Syllabus
Audit Course - II
AC203HS: Stress Management by Yoga

Course Objectives

1. To achieve overall health of body and mind To overcome stress

Course Outcomes

1. Develop healthy mind in a healthy body thus improving social health also Improve efficiency

Unit - I

Definitions of Eight parts of yog. (Ashtanga)

Unit - II

Yam and Niyam.

Unit - III

Dos and Don'ts in life.

i) Ahinsa, satya, astheya, bramhacharya and aparigraha ii) Shaucha, santosh, tapa, swadhyay, ishwarpranidhan

Unit - IV

Asan and Pranayam

Unit - V

i) Various yoga poses and their benefits for mind & body ii) Regularization of breathing techniques and its effects-Types of pranayam

Suggested Readings:

1. "Yogic Asanas for Group Tarining-Part-I": Janardan Swami Yogabhyasi Mandal, Nagpur

Reference Books:

1. "Rajayoga or conquering the Internal Nature" by Swami Vivekananda, Advaita Ashrama (Publication Department), Kolkata.

L	T	P	C
2	0	0	0

M.Tech. in Digital Electronics and Communication Engineering
II Semester Syllabus
Audit Course - II
AC204HS: Personality Development through Life Enlightenment Skills

Course Objectives

1. To learn to achieve the highest goal happily
2. To become a person with stable mind, pleasing personality and determination
3. To awaken wisdom in students

Course Outcomes

1. Study of Shrimad-Bhagwad-Geeta will help the student in developing his personality and achieve the highest goal in life
2. The person who has studied Geeta will lead the nation and mankind to peace and prosperity
3. Study of Neetishatakam will help in developing versatile personality of students

Unit - I

Neetisatakam-Holistic development of personality

- Verses-19, 20, 21, 22 (wisdom)
- Verses-29, 31, 32 (pride & heroism)
- Verses-26, 28, 63, 65 (virtue)

Unit - II

Neetisatakam-Holistic development of personality

- Verses-52, 53, 59 (don'ts)
- Verses-71, 73,75,78 (dos)

Unit - III

Approach to day to day work and duties.

- Shrimad Bhagwad Geeta: Chapter 2-Verses 41, 47, 48,
- Chapter 3-Verses 13, 21, 27, 35, Chapter 6-Verses 5, 13, 17, 23, 35,
- Chapter 18-Verses 45, 46, 48.

Unit-IV

Statements of basic knowledge.

- Shrimad Bhagwad Geeta: Chapter2-Verses 56, 62, 68
- Chapter 12 -Verses 13, 14, 15, 16, 17, 18
- Personality of Role model. Shrimad Bhagwad Geeta:

Unit-V

- Chapter2-Verses 17, Chapter 3-Verses 36, 37, 42,
- Chapter 4-Verses 18, 38, 39
- Chapter18 –Verses 37, 38, 63

Suggested Readings:

1. "Srimad Bhagavad Gita" by Swami Swarupananda Advaita Ashram (Publication Department), Kolkata.
2. Bhartrihari‟s Three Satakam (Niti-sringar-vairagya) by P.Gopinath, Rashtriya Sanskrit Sansthanam, New Delhi.

L	T	P	C
0	0	4	2

M.Tech. in Digital Electronics and Communication Engineering
II Semester Syllabus
EC251PC: ARM Microcontrollers and Programmable Digital Signal Processors Laboratory

Course Objectives

Students undergoing this course are expected to
1. To compare the features of ARM Cortex M3 and DSP C6748.
2. To experiment with the programming of ARM Cortex M3 and DSP C6748.
3. To utilize the instruction set of ARM Cortex M3.
4. To interpret the instruction set of DSP C6748.

Course Outcomes

1. Define and label the instruction sets of Cortex-M3 and TMS320C6748 DSP processors.
2. Classify and configure the instruction sets for Cortex-M3 and TMS320C6748 DSP processors, and outline the codes for application development.
3. Develop prototype code for on-chip and off-chip peripherals on Cortex-M3 development boards using the Keil ARM IDE tool.
4. Build prototype code for on-chip and off-chip peripherals on TMS320C6748 development boards using the CCS IDE tool.
5. Analyze the various peripherals interfacing with the Cortex-M3 processor.
6. Develop and implement codes for mathematical operations and filtering applications using TMS320C6748 DSP processor with CCS tool

Course Articulation Matrix

COs	PO1	PO2	PO3	PO4	PO5	PO6
CO1	2	3	2	2	2	1
CO2	2	3	2	3	3	1
CO3	2	3	2	3	3	2
CO4	2	3	2	3	3	2
CO5	2	3	3	3	3	2
CO6	2	3	3	3	3	2

Note:
Minimum 10 experiments must perform.

List of Experiments:

PART-A

(Part- A experiments to be carried out on Cortex-M3 development boards and using GNU tool chain)

Code Development for Part A:

1. Blink an LED with software delay, delay generated using the SysTick timer.
2. Using the PLL modules with System clock real time alteration.
3. Control intensity of an LED using PWM implemented in software and hardware.
4. Control an LED using switch by polling method, by interrupt method and flash the LED once every five switch presses.
5. UART Echo Test.

6. To take analog readings on rotation of rotary potentiometer connected to an ADC channel for temperature indication on an RGB LED.
7. To mimic light intensity sensed by the light sensor by varying the blinking rate of an LED.
8. To evaluate the various sleep modes by putting core in sleep and deep sleep modes.
9. System reset using watchdog timer in case something goes wrong.
10. To sample sound using a microphone and display sound levels on LEDs.
11. To display date and time using internal Real-Time Clock (RTC) programming.
12. To interface audio controller with Cortex-M3 based microcontroller.
13. To interface GSM module with Cortex-M3 based microcontroller.
14. To interface GPS module with Cortex-M3 based microcontroller.

Part- B

(Part- B experiments to be carried out on DSP C6748 evaluation kits and using Code Composer Studio (CCS))

1. To develop and implement in assembly code and C code to compute Euclidian distance between any two points.
2. To develop and implement in assembly code and study the impact of parallel, serial and mixed execution.
3. To develop and implement in assembly and C code for implementation of convolution operation.
4. To design and implement filters in C to enhance the features of given input sequence/signal.

L	T	P	C
0	0	4	2

M.Tech. in Digital Electronics and Communication Engineering
II Semester Syllabus
EC252PC: Advanced Communications and Networks Laboratory

Course Objectives

The objectives of this course are to make the student
1. To acquire the knowledge in Orthogonal Frequency Division Multiplexing and Spread Spectrum Communications.
2. To study the MIMO Systems.
3. To study the various Wireless LANs and PANs.

Course Outcomes

At the end of this course students will be able to
1. Understand the concepts of Orthogonal Frequency Division Multiplexing and Spread Spectrum Communications.
2. Understand the concepts MIMO Systems
3. Acquire the knowledge of different Wireless LANs and PANs.

Course Articulation Matrix

COs	PO1	PO2	PO3	PO4	PO5	PO6
CO1	-	2	3	3	-	-
CO2	2	2	3	3	2	-
CO3	2	2	2	2	-	-

Note: Below experiment perform using MATLAB

List of Experiments:

1. Implementation of Matched Filters.
2. Optimum receiver for the AWGN channel.
3. Design FIR (LP/HP/BP) filter using Window method.
4. Measurement of effect of Inter Symbol Interference.
5. Generation of constant envelope PSK signal wave form for different values of M.
6. Simulation of PSK system with M=4
7. Simulation of DPSK system with M=4
8. Design of FSK system
9. Simulation of correlation type demodulation for FSK signal
10. BPSK Modulation and Demodulation techniques
11. QPSK Modulation and Demodulation techniques
12. DQPSK Modulation and Demodulation techniques.
13. 8-QAM Modulation and Demodulation techniques.
14. DQAM Modulation and Demodulation techniques.
15. Verification of Decimation and Interpolation of a given signal.
16. Power spectrum estimation using AR models.

L	T	P	C
3	0	0	3

M.Tech. in Digital Electronics and Communication Engineering
III Semester Syllabus
Professional Elective-V
EC311PE: MIMO Systems

Prerequisites: Wireless Communications

Course Objectives

1. To understand basic requirement of MIMO systems.
2. To develop channel modeling for MIMO systems.
3. To calculate capacity for MIMO systems.
4. To study multiplexing capabilities and architectures of MIMO systems.

Course Outcomes

After completion of the course the student should be able to

1. CO1 Describe Basic Features of Coherent and No coherent Detection, Fading and Nonfading Channels and their Capacities, Diversity Techniques and Space-Time Codes.
2. CO2 Differentiate Between Different MIMO Configuration Systems, and Interpret Multi Symbol Transmission using Spatial Multiplexing and Channel Modeling.
3. CO3 Calculate Channel Capacities of Various Fading and Nonfading Channels in MIMO Systems and Interpret the Effects of Diversity Techniques.
4. CO4 Analyze the V-BLAST and D-BLAST Types of Architectures and to Compare BER and Channel Capacity Estimates.
5. CO5 Evaluate Performance Characteristic for Multiuser Communication in MIMO Systems under Different Channel Conditions for Uplink and Downlink.

Course Articulation Matrix

COs	PO1	PO2	PO3	PO4	PO5	PO6
CO1	2	-	2	2	2	-
CO2	-	-	2	-	2	-
CO3	-	-	2	-	3	-
CO4	-	-	2	-	2	-
CO5	2	-	2	3	2	-

Unit - I

Point-to-Point Communication: Detection and Diversity Detection in a Rayleigh Fading Channel – Noncoherent Detection, Coherent Detection, From BPSK to QPSK: Exploiting the Degrees of Freedom, Diversity. Time Diversity – Repetition Coding, Time Diversity in GSM. Antenna Diversity – Receiver Diversity, Transmit Diversity - Space-Time Codes, MIMO. Frequency diversity – Basic Concept, Single-Carrier with ISI Equalization, Direct Sequence Spread Spectrum.

Unit - II

Capacity of Wireless Channels AWGN Channel Capacity - Repetition Coding, Packing Spheres. Linear Time Invariant Gaussian Channels, Single Input Multiple Output (SIMO) Channel, Multiple Input Single Output (MISO) Channel, Frequency-Selective Channel. Capacity of Fading Channels – Slow Fading Channel, Receive Diversity, Transmit Diversity, Time and Frequency Diversity, Fast Fading Channel, Transmitter Side Information, Frequency Selective Fading Channels.

Unit - III

Spatial Multiplexing and Channel Modeling Multiplexing Capability of Deterministic MIMO Channels – Capacity via Singular Value Decomposition, Rank and Condition Number. Physical Modeling of MIMO Channels, Line of-Sight SIMO channel, Line-of-Sight MISO channel, Antenna Arrays with only a Line-of-Sight Path, Geographically Separated Antennas, Line-of-Sight Plus One Reflected Path. Modeling of MIMO Fading Channels – Basic Approach, MIMO Multipath Channel, Angular Domain Representation of Signals, Angular Domain Representation of MIMO Channels, Statistical Modeling in the Angular Domain, Degrees of Freedom and Diversity, Dependency on Antenna Spacing, IID Rayleigh Fading Model.

Unit - IV

Capacity and Multiplexing Architectures: The V-BLAST Architecture. Fast fading MIMO Channel – Capacity with CSI at Receiver, Performance Gains, Full CSI. Receiver Architectures – Linear Decorrelator, Successive Cancellation, Linear MMSE Receiver, Information Theoretic Optimality. Slow Fading MIMO Channel. DBLAST: an Outage-Optimal Architecture – Sub-Optimality of V-BLAST, Coding Across Transmit Antennas: DBLAST.

Unit - V

Multiuser Communication: Uplink with Multiple Receive Antennas – Space-Division Multiple Access, SDMA Capacity Region, System Implications, Slow Fading, Fast Fading, Multiuser Diversity Revisited. MIMO uplink – SDMA with Multiple Transmit Antennas, System Implications, Fast Fading. Downlink with Multiple Transmit Antennas, Degrees of Freedom in the Downlink.

Text Books:

1. David Tse, and Pramod Viswanath, "Fundamentals of Wireless Communication", 1st edition, Cambridge University Press, 2014.
2. Mohinder Janakiraman, "Space - Time Codes and MIMO Systems", Artech House Publishers, 2004.

Reference Books:

1. Claude Oestges, and Bruno Clerckx, "MIMO Wireless Communications: From Real-world Propagation to Space-time Code Design", Academic Press, 1st edition, 2010.
2. Togla M. Duman, and Ali Ghrayeb, "Coding for MIMO Communication Systems", John Wiley & Sons Ltd, 2007.
3. Hamid Jafarkhani, "Space Time coding –Theory and Practice", Cambridge university press, 2005.

Online Resource:

http://nptel.ac.in/courses/117105132/

(**Course Title:** Fundamentals of MIMO Wireless Communication, Prof. Surva Sekhar Das, IIT Kharagpur)

L	T	P	C
3	0	0	3

M.Tech. in Digital Electronics and Communication Engineering
III Semester Syllabus
Professional Elective - V
EC312PE: System on Chip Architecture

Course Objectives

The objectives of this course are to make the student
1. To design, optimize, and program a modern System-on-a-Chip.
2. To (i) analyze a computational task, (ii) characterize its computational requirements, (iii) identify performance bottlenecks, (iv) identify, explore, and evaluate a rich design space of solutions, and (v) select and implement a design that meets engineering requirements.

Course Outcomes

By the end of the course, the students will be able to:
1. Decompose the task into parallel components that cooperate to solve the problem.
2. Characterize and develop real-time solutions.
3. Implement both hardware and software solutions, formulate hardware/software tradeoffs, and perform hardware/software code sign.
4. Understand the system on a chip from gates to application software, including on-chip memories and communication networks, I/O interfacing, RTL design of accelerators, processors, firmware and OS/infrastructure software.
5. Understand and estimate key design metrics and requirements including area, latency, throughput, energy, power, predictability, and reliability.

Course Articulation Matrix

COs	PO1	PO2	PO3	PO4	PO5	PO6
CO1	3	-	2	2	3	-
CO2	2	-	2	2	2	2
CO3	2	-	2	3	3	-
CO4	2	-	3	3	2	-
CO5	-	-	2	-	3	-

Unit - I

Introduction to the System Approach: System Architecture, Components of the system, Hardware & Software, Processor architectures, Memory and Addressing, System level interconnection, An approach for SOC Design, System Architecture and Complexity.

Unit - II

Processors: Introduction, Processor Selection for SOC, Basic concepts in Processor Architecture, Basic concepts in Processor Micro Architecture, Basic elements in Instruction handling. Buffers: minimizing Pipeline Delays, Branches, More Robust Processors, Vector Processors and Vector Instructions extensions, VLIW Processors, Superscalar Processors.

Unit - III

Memory Design for SOC: Overview of SOC external memory, Internal Memory, Size, Scratchpads and Cache memory, Cache Organization, Cache data, Write Policies, Strategies for line replacement at miss time, Types of Cache, Split – I, and D – Caches, Multilevel Caches, Virtual to real translation, SOC Memory System, Models of Simple Processor – memory interaction.

Unit - IV

Interconnect Customization and Configuration: Inter Connect Architectures, Bus: Basic Architectures, SOC Standard Buses, Analytic Bus Models, Using the Bus model, Effects of Bus transactions and contention time. SOC Customization: An overview, Customizing Instruction Processor, Reconfiguration Technologies, Mapping design onto Reconfigurable devices, Instance- Specific design, Customizable Soft Processor, Reconfiguration - overhead analysis and trade-off analysis on reconfigurable Parallelism.

Unit - V

Application Studies / Case Studies: SOC Design approach, AES algorithms, Design and evaluation, Image compression – JPEG compression.

Suggested Readings:

1. Michael J. Flynn and Wayne Luk, Computer System Design System-on-Chip, Wiely India Pvt. Ltd.
2. Steve Furber, ARM System on Chip Architecture, Addison Wesley Professional. 2nd Eed., 2000

Reference Books:

1. Ricardo Reis, Design of System on a Chip: Devices and Components, 1st Ed., Springer, 2004.
2. Jason Andrews, Co-Verification of Hardware and Software for ARM System on Chip Design (Embedded Technology) , Newnes, BK and CDROM
   Prakash Rashinkar, Peter Paterson and Leena Singh L, System on Chip Verification Methodologies and Techniques, Kluwer Academic Publishers, 2001.

L	T	P	C
3	0	0	3

M.Tech. in Digital Electronics and Communication Engineering
III Semester Syllabus
Professional Elective - V
EC313PE: Embedded Networking

Prerequisites: Embedded Systems.

Course Objectives

1. To understand the wired and wireless embedded communication protocols.
2. To study the basics of Ethernet and embedded Ethernet.
3. To discuss the wireless embedded networking protocols.
4. To infer the issues in networked embedded system development.

Course Outcomes

After completion of the course the students should be able to

1. Narrate the features of embedded networking, basics of Ethernet communication and outline the serial, parallel, and wireless communication protocols.
2. Distinguish between USB and CAN bus protocols for embedded system applications.
3. Implement the TCP and UDP protocols for client and server model in networked embedded systems.
4. Apply the wireless protocols in real world interfacing.
5. Develop a networked embedded system for real time applications.

Course Articulation Matrix

COs	PO1	PO2	PO3	PO4	PO5	PO6
CO1	-	-	2	3	2	-
CO2	2	-	3	2	3	-
CO3	2	-	3	3	2	-
CO4	2	-	3	2	2	2
CO5	2	-	3	3	2	2

Unit - I

Embedded Communication Protocols: Embedded Networking: Introduction– Serial/Parallel Communication–Serial Communication Protocols-RS232 standard–RS485–Synchronous Serial Protocols-Serial Peripheral Interface (SPI)–Inter Integrated Circuits (I2C)–PC Parallel port programming–ISA/PCI Bus protocols–Fire wire.

Unit - II

USB and CAN Bus: USB bus–Introduction–Speed Identification on the bus– USB States–USB bus communication: Packets–Data flow type–Enumeration–Descriptors–PIC 18 Microcontroller USB Interface–C Programs–CAN Bus–Introduction–Frames–Bit stuffing–Types of errors–Nominal Bit Timing–PIC microcontroller CAN Interface– A simple application with CAN.

Unit - III

Ethernet Basics: Elements of a network–Inside Ethernet–Building a Network: Hardware options–Cables, Connections and network speed–Design choices: Selecting components–Ethernet Controllers–Using the internet in local and internet communications–Inside the internet protocol.

Unit - IV

Embedded Ethernet: Exchanging messages using UDP and TCP–Serving web pages with Dynamic Data– Serving web pages that respond to user Input–Email for Embedded Systems–Using FTP–Keeping Devices and Network secure.

Unit - V

Wireless Embedded Networking: Wireless sensor networks–Introduction– Applications–Network Topology–Localization–Time Synchronization–Energy efficient MAC protocols–SMAC–Energy efficient and robust routing–Data Centric routing.

Text Books:

1. K.V. Sibhu, "Introduction to Embedded Systems", 2nd Edition, 2017.
2. Jan Axelson, "Embedded Ethernet and Internet Complete", Penram Publications, 2003.
3. Bhaskar Krishnamachari, Networking Wireless Sensors", Cambridge press 2005.

Reference Books:

1. Dogan Ibrahim, "Advanced PIC microcontroller projects in C: from USB to RTOS with the PIC18F series", Elsevier 2008.
2. Jan Axelson, "Parallel Port Complete: Programming, interfacing and using the PCs parallel printer port",Penram Publications, 1996.
3. Frank Vahid, Tony Givargis, "Embedded Systems Design: A Unified Hardware/Software Introduction", John & Wiley Publications, 2002.
4. Dawoud Shenouda Dawoud and Peter Dawoud, "Serial Communication Protocols and Standards", River Publications, July 2020.
5. Dawoud Shenouda Dawoud and Peter Dawoud, "Microcontroller and Smart Home Networks", River Publications, July 2020.

Online Resources:

1. http://www.infocobuild.com/education/audio-video-courses/electronics/EmbeddedSystems-IIT-Delhi/ lecture-24.html (Course Title: Embedded systems by Prof. SantanuChaudhury, IIT Delhi)
2. https://nptel.ac.in/courses/108102045 (Course Title: Embedded systems by Prof. SantanuChaudhury, IIT Delhi)
3. http://www.nitttrc.edu.in/nptel/courses/video/108102045/lec1.pdf(Tutorials on Embedded systems by Prof. SantanuChaudhury, IITDelhi)
4. http://kishorekumarbooks.blogspot.com/2019/04/embedded-networking-notes.html (Tutorials on Embedded Networking)

L	T	P	C
3	0	0	3

M.Tech. in Digital Electronics and Communication Engineering
III Semester Syllabus
Open Elective
EC321OE: System on Chip Architecture

Prerequisites: Embedded Systems.

Course Objectives

The objectives of this course are to make the student
1. To design, optimize, and program a modern System-on-a-Chip.
2. To (i) analyze a computational task, (ii) characterize its computational requirements, (iii) identify performance bottlenecks, (iv) identify, explore, and evaluate a rich design space of solutions, and (v) select and implement a design that meets engineering requirements.

Course Outcomes

By the end of the course, the students will be able to:
1. Decompose the task into parallel components that cooperate to solve the problem.
2. Characterize and develop real-time solutions.
3. Implement both hardware and software solutions, formulate hardware/software tradeoffs, and perform hardware/software code sign.
4. Understand the system on a chip from gates to application software, including on-chip memories and communication networks, I/O interfacing, RTL design of accelerators, processors, firmware and OS/infrastructure software.
5. Understand and estimate key design metrics and requirements including area, latency, throughput, energy, power, predictability, and reliability.

Course Articulation Matrix

COs	PO1	PO2	PO3	PO4	PO5	PO6
CO1	3	-	2	2	2	2
CO2	-	-	2	2	2	-
CO3	-	-	2	3	3	-
CO4	2	-	2	2	3	2
CO5	-	-	2	-	3	-

Unit - I

Introduction to the System Approach: System Architecture, Components of the system, Hardware & Software, Processor architectures, Memory and Addressing, System level interconnection, An approach for SOC Design, System Architecture and Complexity.

Unit - II

Processors: Introduction, Processor Selection for SOC, Basic concepts in Processor Architecture, Basic concepts in Processor Micro Architecture, Basic elements in Instruction handling. Buffers: minimizing Pipeline Delays, Branches, More Robust Processors, Vector Processors and Vector Instructions extensions, VLIW Processors, Superscalar Processors.

Unit - III

Memory Design for SOC: Overview of SOC external memory, Internal Memory, Size, Scratchpads and Cache memory, Cache Organization, Cache data, Write Policies, Strategies for line replacement at miss time, Types of Cache, Split – I, and D – Caches, Multilevel Caches, Virtual to real translation, SOC Memory System, Models of Simple Processor – memory interaction.

Unit - IV

Interconnect Customization and Configuration: Inter Connect Architectures, Bus: Basic Architectures, SOC Standard Buses, Analytic Bus Models, Using the Bus model, Effects of Bus transactions and contention time. SOC Customization: An overview, Customizing Instruction Processor, Reconfiguration Technologies, Mapping design onto Reconfigurable devices, Instance- Specific design, Customizable Soft Processor, Reconfiguration - overhead analysis and trade-off analysis on reconfigurable Parallelism.

Unit - V

Application Studies / Case Studies: SOC Design approach, AES algorithms, Design and evaluation, Image compression – JPEG compression.

Suggested Readings:

1. Michael J. Flynn and Wayne Luk, Computer System Design System-on-Chip, Wiely India Pvt. Ltd.
2. Steve Furber, ARM System on Chip Architecture, Addison Wesley Professional. 2nd Eed., 2000

Reference Books:

1. Ricardo Reis, Design of System on a Chip: Devices and Components, 1st Ed., Springer, 2004.
2. Jason Andrews, Co-Verification of Hardware and Software for ARM System on Chip Design (Embedded Technology) , Newnes, BK and CDROM
   Prakash Rashinkar, Peter Paterson and Leena Singh L, System on Chip Verification Methodologies and Techniques, Kluwer Academic Publishers, 2001.

L	T	P	C
3	0	0	3

M.Tech. in Digital Electronics and Communication Engineering
III Semester Syllabus
Open Elective
EC322OE: Cognitive Radio

Course Objectives

The objectives of this course are to make the student
1. To provide an overview and Function of Cognitive Radios.
2. To provide clear understanding about the Dynamic Spectrum Allocation, Spectrum Access and Management.
3. To provide knowledge about the Spectrum Trading.
4. To understand the Research Challenges in Cognitive Radio.

Course Outcomes

At the end of this course, students will be able to Understand the fundamental concepts of cognitive radio networks.
1. Develop the cognitive radio, as well as techniques for spectrum holes detection that cognitive radio takes advantages in order to exploit it.
2. Understand technologies to allow an efficient use of TVWS for radio communications based on two spectrum sharing business models/policies.
3. Understand fundamental issues regarding dynamic spectrum access, the radio-resource management and trading, as well as a number of optimization techniques for better spectrum exploitation.

Course Articulation Matrix

COs	PO1	PO2	PO3	PO4	PO5	PO6
CO1	2	-	2	3	2	-
CO2	-	-	2	3	3	-
CO3	3	-	3	3	3	2

Unit - I

Introduction to Cognitive Radios: Digital dividend, cognitive radio (CR) architecture, functions of cognitive radio, dynamic spectrum access (DSA), components of cognitive radio, spectrum sensing, spectrum analysis and decision, potential applications of cognitive radio.

Unit - II

Spectrum Sensing: Spectrum sensing, detection of spectrum holes (TVWS), collaborative sensing, geo-location database and spectrum sharing business models (spectrum of commons, real time secondary spectrum market).

Unit - III

Optimization Techniques of Dynamic Spectrum Allocation: Linear programming, convex programming, nonlinear programming, integer programming, dynamic programming, stochastic programming.

Unit - IV

Dynamic Spectrum Access and Management: Spectrum broker, cognitive radio architectures, centralized dynamic spectrum access, distributed dynamic spectrum access, learning algorithms and protocols.

Unit - V

Spectrum Trading: Introduction to spectrum trading, classification to spectrum trading, radio resource pricing, brief discussion on economics theories in DSA (utility, auction theory), and classification of auctions (single auctions, double auctions, concurrent, sequential). Research Challenges in Cognitive Radio: Network layer and transport layer issues, cross layer design for cognitive radio networks.

Suggested Readings:

1. Ekram Hossain, Dusit Niyato, Zhu Han, "Dynamic Spectrum Access and Management in Cognitive Radio Networks", Cambridge University Press, 2009.

Reference Books:

1. Kwang-Cheng Chen, Ramjee Prasad, "Cognitive radio networks", John Wiley & Sons Ltd., 2009.
2. Bruce Fette, "Cognitive radio technology", Elsevier, 2nd edition, 2009.
3. Huseyin Arslan, "Cognitive Radio, Software Defined Radio, and Adaptive Wireless Systems", Springer, 2007.
4. Francisco Rodrigo Porto Cavalcanti, Soren Andersson, "Optimizing Wireless Communication Systems" Springer, 2009. 5. Linda Doyle, "Essentials of Cognitive Radio", Cambridge University Press, 2009.

L	T	P	C
3	0	0	3

M.Tech. in Digital Electronics and Communication Engineering
III Semester Syllabus
Open Elective
EC323OE: IOT and its Applications

Course Objectives

The objectives of this course are to make the student
1. To study the fundamentals of IOT and M2M.
2. To study the reference models of IOT.
3. Study the security and privacy issues in IOT.

Course Outcomes

At the end of this course, students will be able to:
1. Understand the concept of IOT and M2M
2. Study IOT architecture and applications in various fields
3. Study the security and privacy issues in IOT

Course Articulation Matrix

COs	PO1	PO2	PO3	PO4	PO5	PO6
CO1	2	-	2	2	-	-
CO2	2	-	2	2	2	2
CO3	2	-	2	3	2	-

Unit - I

IoT & Web Technology The Internet of Things Today, Time for Convergence, Towards the IoT Universe, Internet of Things Vision, IoT Strategic Research and Innovation Directions, IoT Applications, Future Internet Technologies, Infrastructure, Networks and Communication, Processes, Data Management, Security, Privacy & Trust, Device Level Energy Issues, IoT Related Standardization, Recommendations on Research Topics.

Unit - II

M2M to IoT – A Basic Perspective– Introduction, Some Definitions, M2M Value Chains, IoT Value Chains, An emerging industrial structure for IoT, The international driven global value chain and global information monopolies. M2M to IoT-An Architectural Overview– Building an architecture, Main design principles and needed capabilities, An IoT architecture outline, standards considerations.

Unit - III

IoT Architecture -State of the Art – Introduction, State of the art, Architecture Reference Model- Introduction, Reference Model and architecture, IoT reference Model, IoT Reference Architecture- Introduction, Functional View, Information View, Deployment and Operational View, Other Relevant architectural views.

Unit - IV

IoT Applications for Value Creations Introduction, IoT applications for industry: Future Factory Concepts, Brownfield IoT, Smart Objects, Smart Applications, Four Aspects in your Business to Master IoT, Value Creation from Big Data and Serialization, IoT for Retailing Industry, IoT For Oil and Gas Industry, Opinions on IoT Application and Value for Industry, Home Management, eHealth.

Unit - V

Internet of Things Privacy, Security and Governance Introduction, Overview of Governance, Privacy and Security Issues.

Suggested Readings:

1. Vijay Madisetti and Arshdeep Bahga, "Internet of Things (A Hands-on-Approach)", 1st Edition, VPT, 2014.
2. Francis daCosta, "Rethinking the Internet of Things: A Scalable Approach to Connecting Everything", 1st Edition, Apress Publications, 2013.
3. Cuno Pfister, "Getting Started with the Internet of Things", O Reilly Media, 2011.